



PL/X Series Digital DC Drive

Stack Driver Product Manual

Version 5.1+ Software

HG501596 J

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IMPORTANT

This document is a supplement to the *PL/X Series Digital DC Drive Product Manual* (Bardac Manual HG501441) and the *PL/X Technical Manual Addendum - Application Software* (Bardac Manual HG501442).

Please read and fully understand the contents of this manual before installing or commissioning your drive. If in doubt about any sections of this manual, before proceeding, please call Bardac Drives for assistance at:

410-604-3400

Bardac **drives**



NOTE. These instructions do not purport to cover all details or variations in equipment, or to provide for every possible contingency to be met in connection with installation, operation, or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the local Supplier sales office. The contents of this instruction manual shall not become part of or modify any prior or existing agreement, commitment, or relationship. The sales contract contains the entire obligation of Bardac Drives. The warranty contained in the contract between the parties is the sole warranty of Bardac Drives. Any statements contained herein do not create new warranties or modify the existing warranty.

IMPORTANT MESSAGE. This is a version 5.15 PL/XD Stack Driver manual. Units that are installed with version 5.17 upward software have all the functions described. For units that are installed with previous software versions, please refer to the record of modifications at the back of the manual to confirm functionality differences.

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This manual should be used with the main PL / PLX Digital DC Drive product manual.

IMPORTANT. Please see WARNINGS in the main PL / PLX Digital DC Drive product manual.

2 Introduction

The PL/XD is used for controlling external 3 phase thyristor stacks for DC motors, (also slip ring motors) and possesses all the functionality of the PL/X range. It is in the same package as the PL/X 5 - 50 models. Comprehensive details are included in this manual to assist the user in designing the external interface. The PL/XD provides gate drive pulses for driving **user supplied pulse transformers** with primary pulse current up to 1.5 Amp. See also 13 Pulse transformer unit (LA102800).

There are terminals to accept an **externally generated isolated armature current signal**, field signal, thermal heatsink sensor switch, and high voltage armature voltage feedback.

The unit also provides a +24V supply for the gate drive pulse transformers that is short circuit protected.

The following stack configurations can be driven by the PL/XD.

- 1) 6 pulse 2 Quadrant bridge (6 thyristors), or 2 bridges in **parallel** (12 thyristors).
 - 2) 6 pulse 4 Quadrant regen **anti parallel** bridge (12 thyristors).
 - 3) Also 2 / 4 quadrant modes for a 5 / 10 device bridge with 3 phase output to drive slip ring motors
- Extra stacks can be used in parallel within the gate drive capability.

All customer control terminals are the plug in screw terminal variety.

The PL/XD can be used with up to 690V AC on its 3 phase auxiliary supply inputs (EL1/2/3). The external stacks can be of higher voltages if required.

The armature voltage inputs can monitor up to +/-1000 Volts DC.

There is an integral motor field bridge with independant single phase AC supply inputs (EF2/3) for controlling fields up to 32A or 50 Amps (model PL/XD50A). The internal field supply input voltage rating is 480V AC.

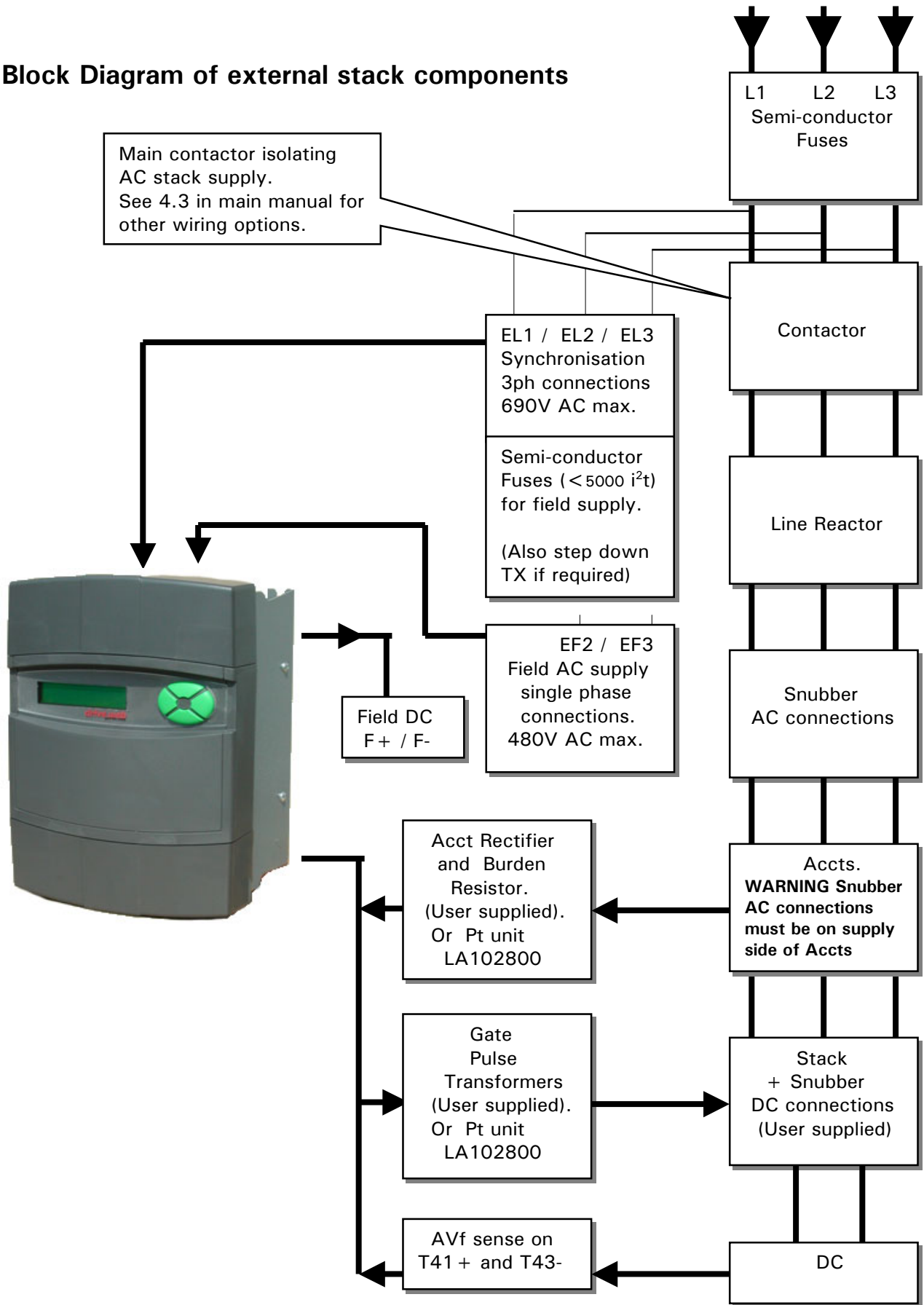
Provision is made for providing an external field feedback signal and controlling an external field with **user supplied primary gate pulse transformer drivers**. See also 13 Pulse transformer unit (LA102800).

All transformer components (pulse tx, acct) that interface with high voltage circuits must have an isolation voltage of at least 4 times AC volts plus 1000V.

Eg for 480 volts AC, isolation voltage rating must be at least 2920 Volts. Also the interwinding capacitance must be as low as possible and not in excess of 10 picofarad between primary and secondary.

There is a **Pulse transformer unit** (Product code LA102800) available at extra cost for users who prefer not to supply their own components. It contains all the external interface components required to combine the PL/XD with the thyristor stack and its associated Accts (AC current transformers). It includes 12 pulse transformer networks for 2 or 4 quadrant bridges, an armature burden rectifier network, and 2 pulse transformer networks for an external field bridge. The unit is designed to be mounted on a DIN rail and all the interface connections are via screw terminals. See 13 Pulse transformer unit (LA102800).

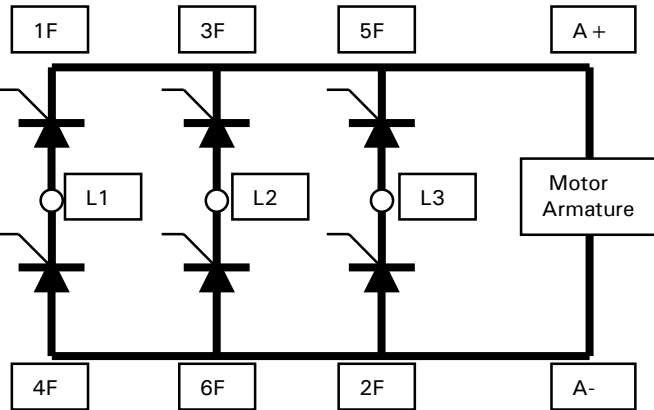
3 Block Diagram of external stack components



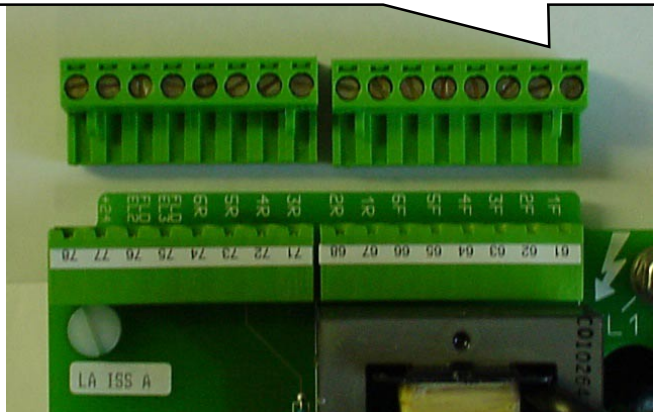
4 Stack Configurations

The stack configuration is set by code switches on the unit. See section 9.2 679)ID ABCXRxxx MON

4.1 Armature bridge 2 quadrant

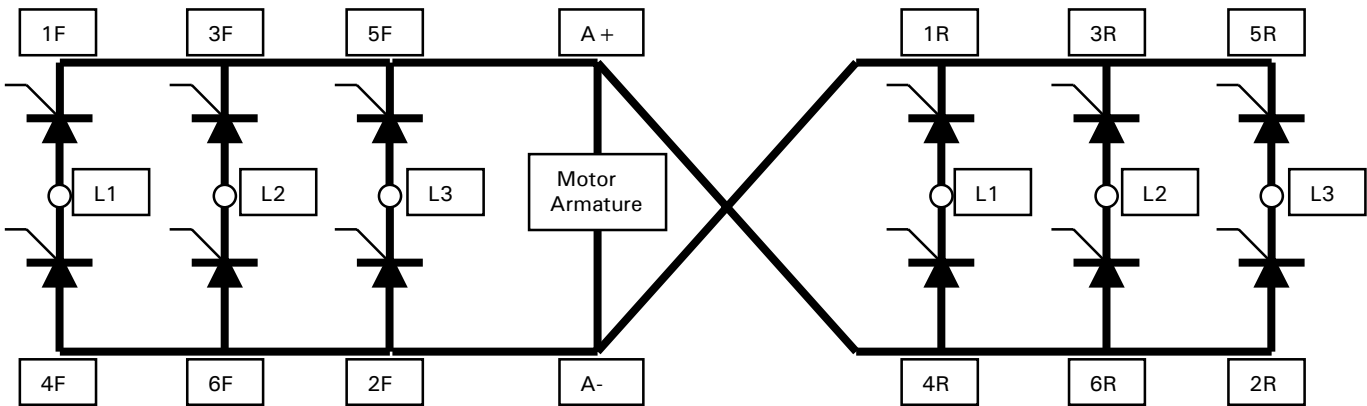


Terminals at top left hand of PL/XD
 T61 62 63 64 65 66 67 68 | 71 72 73 74 75 76 77 78
 1F 2F 3F 4F 5F 6F 1R 2R || 3R 4R 5R 6R Field V+ Fin
 e13 e12
 Terminal 61



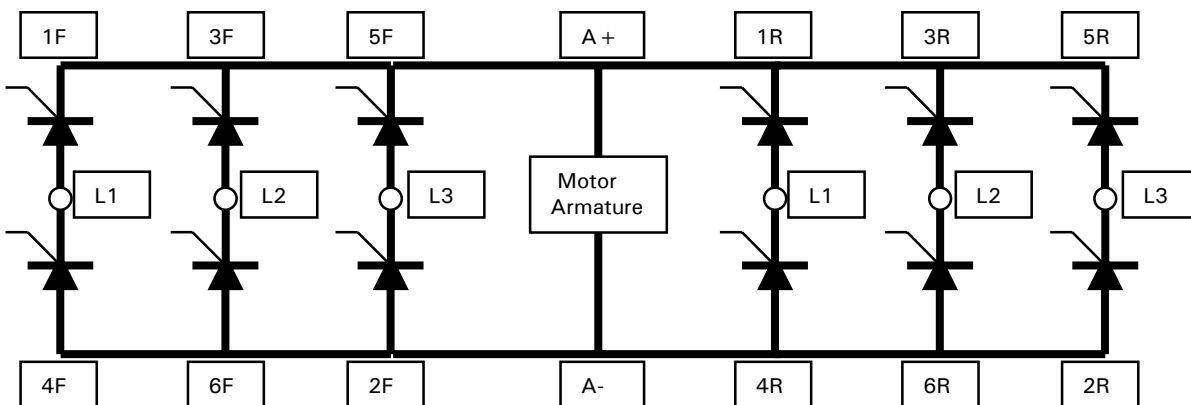
4.2 Armature bridge 4 quadrant

When 4 quadrant mode is selected the R pulses allow firing of an anti-parallel bridge.



4.3 Armature bridge 2 quadrant parallel

When 2 quadrant mode is selected the R pulses change sequence to allow firing of a parallel bridge.



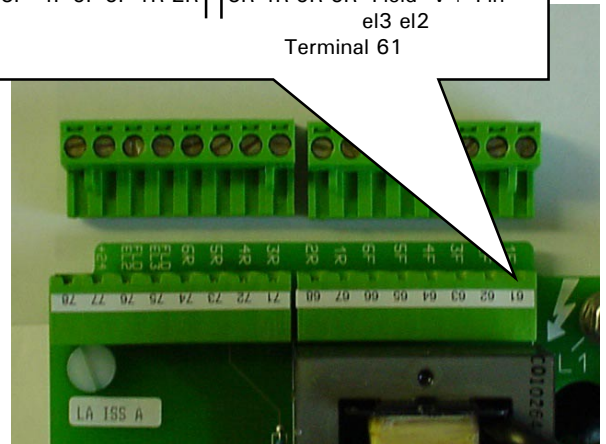
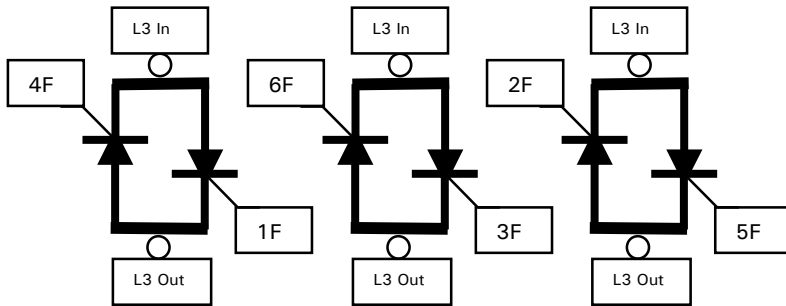
4.4 Slip ring motor single direction

2 quadrant modes

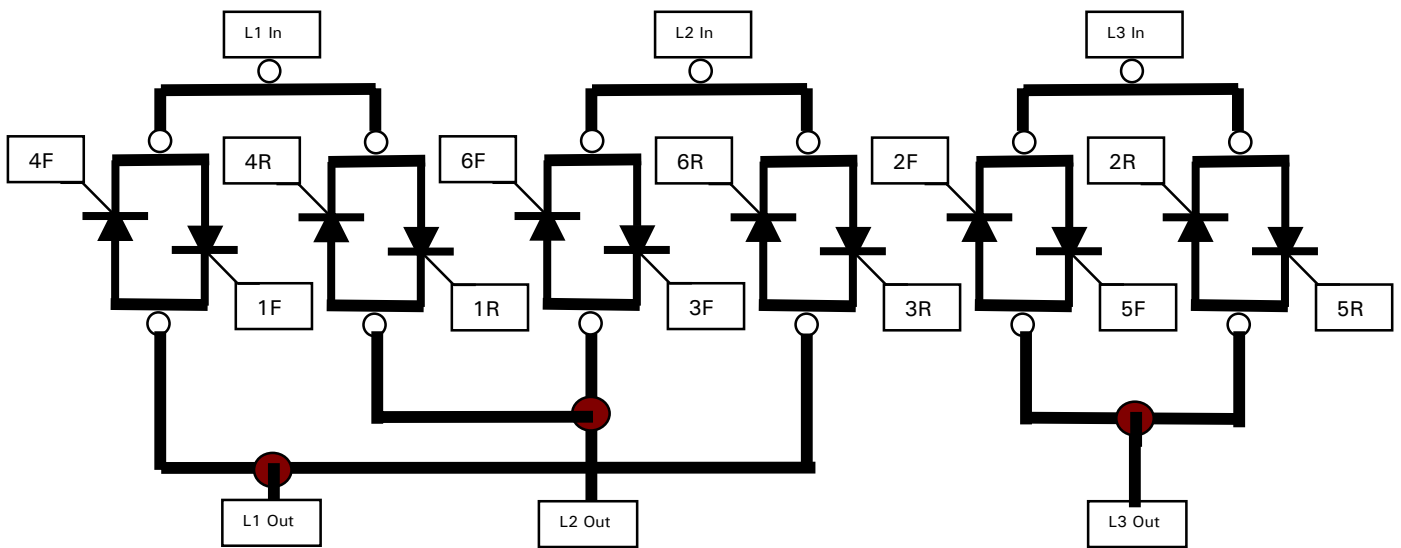
Terminals at top left hand of PL/XD

T61	62	63	64	65	66	67	68	71	72	73	74	75	76	77	78
1F	2F	3F	4F	5F	6F	1R	2R	3R	4R	5R	6R	Field	V+	Fin	
													e13	e12	

 Terminal 61



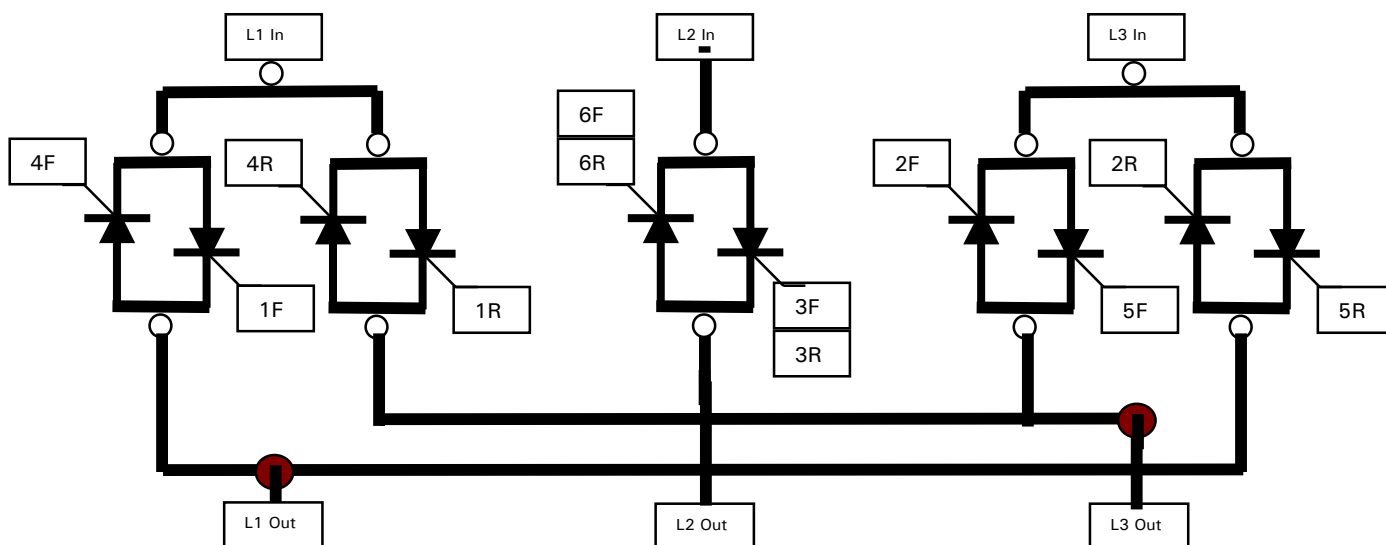
4.5 Slip ring motor bi-directional 4 Quadrant



When 4 quadrant mode is selected the R pulses allow firing of a parallel bridge which introduces phase rotation at the output.

The digital outputs may be used to control relays for connecting dynamic resistors to modify the torque-speed relationship of the motor.

4.6 Slip ring motor bi-directional 4 Quadrant using 10 thyristors



This 4 quadrant configuration saves on 2 thyristors. The 6F and 6R gate outputs must be tied together and used to fire the gate as shown, in the usual way. Similarly the 3F and 3R gate driver outputs must be tied together and used to fire the other gate as shown, in the usual way. The gate outputs are able to be linked because they are open collector.

When 4 quadrant mode is selected the R pulses allow firing of a parallel bridge which introduces phase rotation at the output. The PLX/D will regenerate in both directions of rotation.

The digital outputs may be used to control relays for connecting dynamic resistors to modify the torque-speed relationship of the motor.

4.7 General notes for slip ring motor application

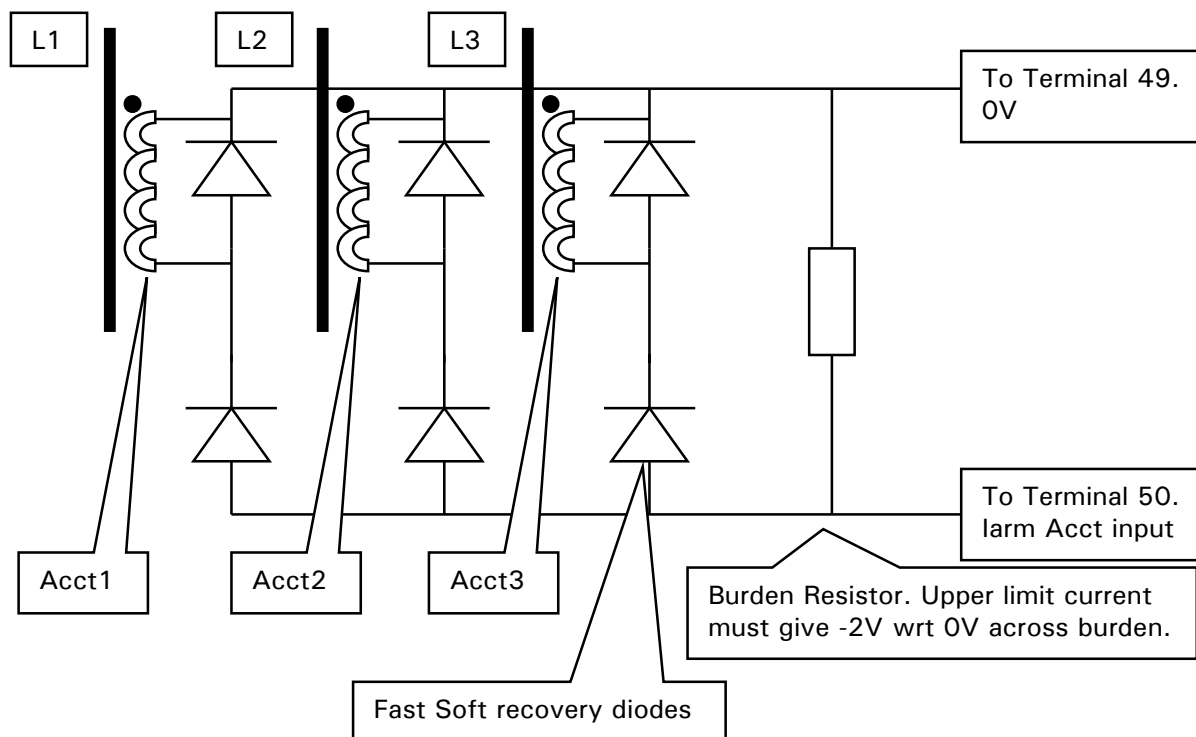
Please refer to the JLX manual HG103521. A copy can be downloaded from www.bardac.com

4.7.1 Slip ring motor recipe configuration

There is a standard slip ring motor recipe configuration available which will allow the PL/XD to provide all the necessary control features for a slip ring motor application. This includes control of the rotor resistors and also crane control with plugging and hyper-synchronous regeneration.

5 Armature Accts

IMPORTANT Make sure the thyristor snubber AC connections are made on the supply side of these Accts. This is to prevent snubber current from external transients being measured by the armature Accts. Make sure the EL1/2/3 and EF2/3 connections are also on the supply side of the armature Accts. This is to prevent the field current being measured by the armature Accts.



This circuit is required externally to generate an armature current signal. The Accts will typically be grain orientated silicon steel. This circuit is able to measure the current waveforms in the AC supply lines to the Stack. By combining the signal from each line through the diode bridge a representation of the armature current is generated across the burden resistor.

You must follow this circuit to ensure that there are no signal distortions due to the magnetisation current of the Accts, and that the polarity of the signal is correct. If you are retro fitting the stack driver to an existing installation with a different wiring scheme for the Acct diode bridge, please reconnect as above.

See 13 Pulse transformer unit (LA102800). This circuit is included on the unit.

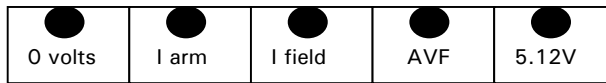
Note. Although there are solutions using only 2 Accts, unless they have special cores, the signal distortions may cause malfunction of the bridge switch logic. This is because of distorted zero crossings of the current waveform. For applications that don't require 4 quadrant control with the PL/XD in PL mode then it may be possible to use a 2 Acct solution, in which case the Acct's are connected between the Phases.

Note. It is important that the mechanical orientation of all three Accts on the Line busbars is the same. (To produce the same sign secondary signal current). This is because the circuit relies on equivalent current polarity from each ACCT. Also the diodes must be fast soft recovery types to prevent commutation distortion of the signal. The average diode current rating must be at least twice the burden current and also have a high peak capability of at least 10 times burden current to survive fault currents. Diode voltage rating 50V min.

See 9.3 How to calibrate the PL/XD armature current.

5.1 Signal test pins

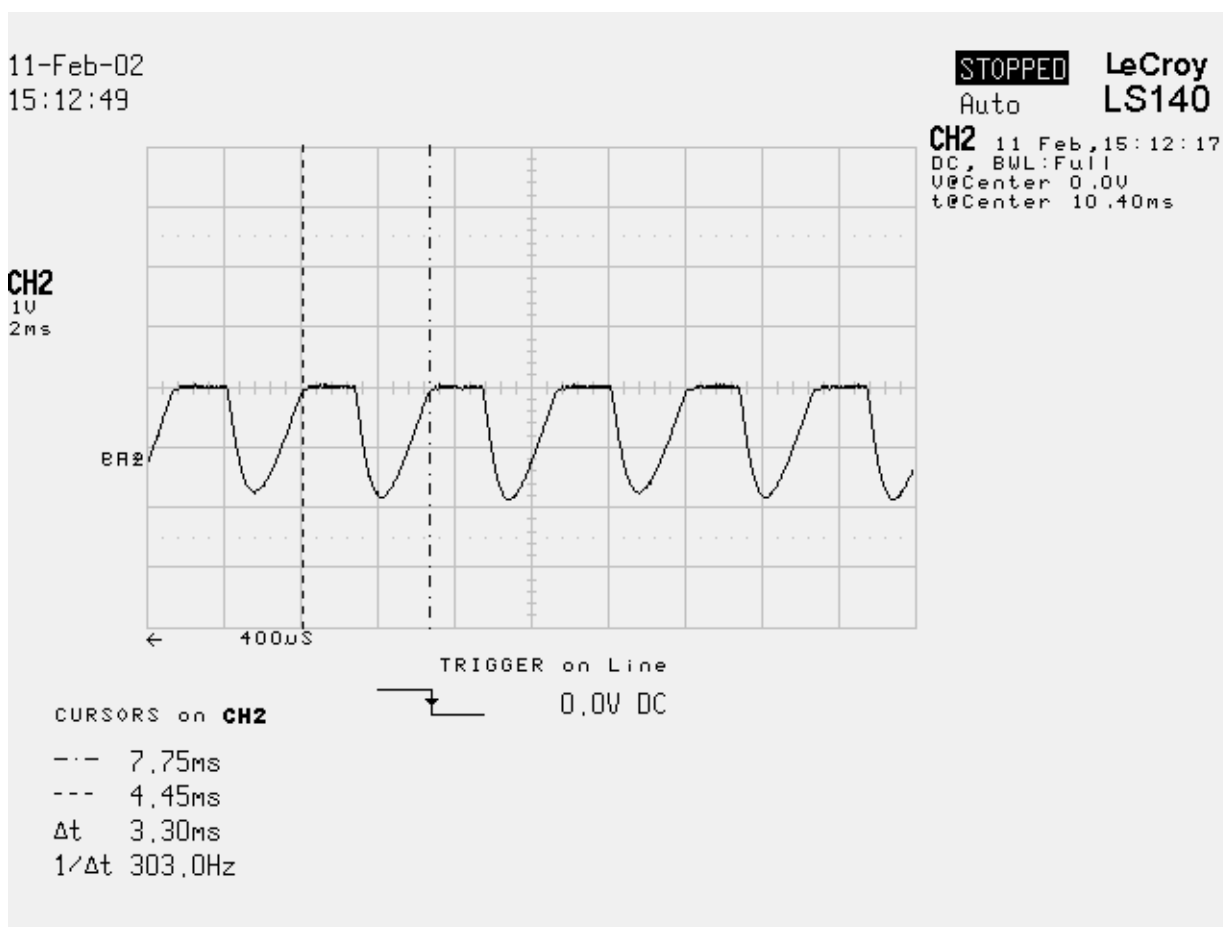
There is a row of test pins just behind the middle control terminal used to monitor certain feedback signals.



The I arm signal is an attenuated unfiltered inverted version of terminal 29, and may be used to observe the current response of the PL/X.

See 250)Iarm OP RECTIFY. This parameter is used to make the current waveform rectified or unrectified. Signal sign and amplitude is 0 to +/- 2V linear output for 0 to +/-100% max stack rating current for unrectified mode, or 0 to -2V linear output for 0 to +/-100% max stack rating current for rectified mode.

Below is a current waveform trace.



This is a discontinuous current waveform trace using Accts of diameter 150 mm, 4000 turns silicon iron grain orientated steel cores. Notice that there are no turn off tails normally associated with such cores. This is because they have been connected as described.

See also 9.3 How to calibrate the PL/XD armature current.

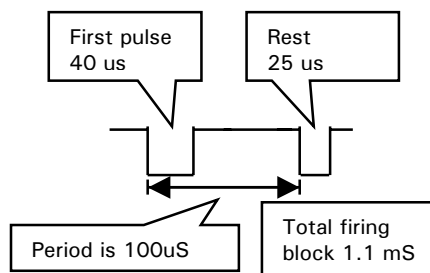
6 Armature thyristor gate waveform

All pulse transformers must have an isolation voltage of at least 4 times AC volts plus 1000V.

Eg for 480 volts AC, isolation voltage rating must be at least 2920 Volts.

Also the interwinding capacitance must be as low as possible and not in excess of 10 picofarad.

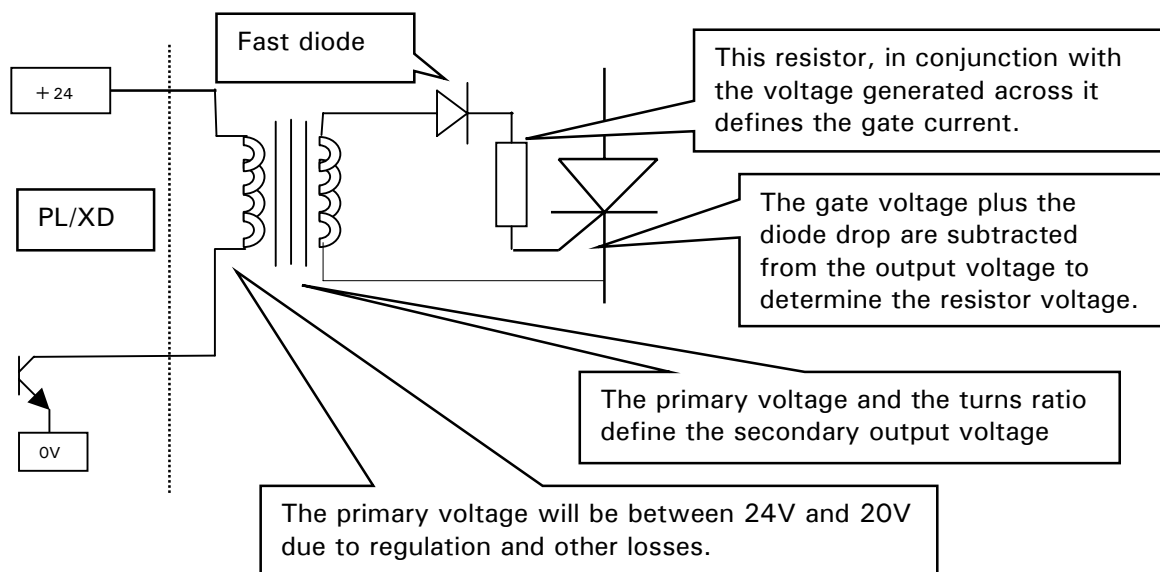
The firing pulse outputs are open collector. The maximum current sinking capability is 1.5 Amps per output. (Note. The Pulse transformer unit LA102800 requires 1.5A per channel. See 13 Pulse transformer unit (LA102800))



6.1 Armature pulse transformer circuit (Voltage driven)

This circuit is quite common but the current drive method discussed in the next section is much better. (The diagram below is a simplistic circuit, there may be other components e.g. gate shorting resistors).

This type of circuit requires a pulse transformer that can support the drive voltage for at least 40 uS (Volt-micro-seconds). In practice there would need to be a large margin of safety to take account of primary voltage and pulse timing tolerances. If the pulse transformer were to saturate due to an insufficient Volt-seconds rating then the primary circuit would be short circuited.



Example. The pulse transformer has a 2 : 1 ratio. The desired minimum gate firing current is 1 amp.

Assume worst case primary voltage of 20V. Hence output secondary voltage will be 10V. The voltage across the resistor will be (10 - diode drop (1V) - gate voltage (2V)) = 7V

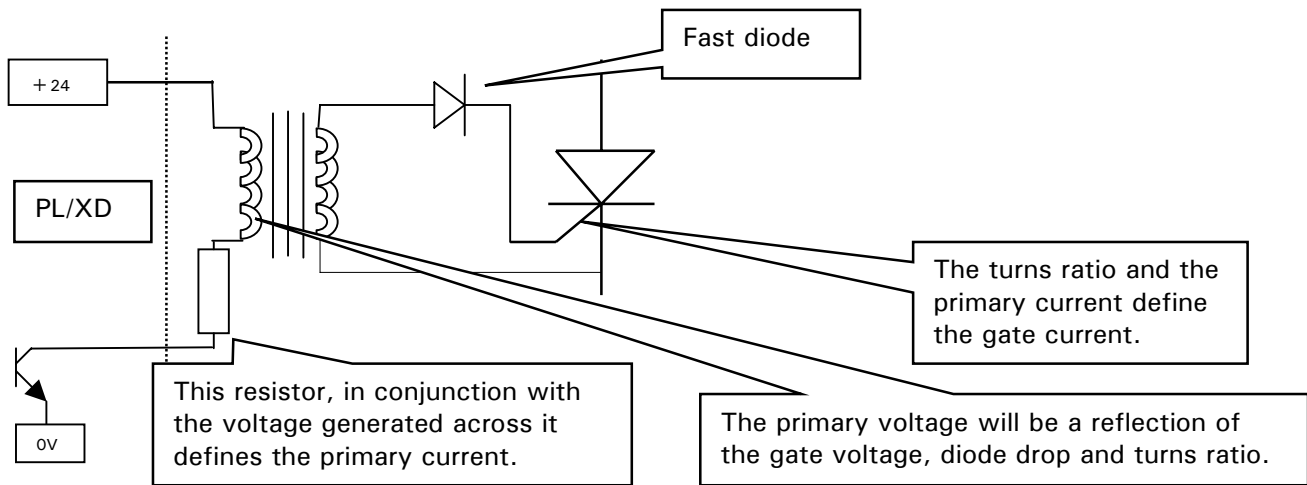
Hence for 1 amp gate current the resistor must be 7 Ohms.

(The peak primary current will be 0.5A). The average primary current is reduced due to the pulse duty cycle (25% X 1.1mS / 3.3mS) and the thyristor duty. (1/3) = a total reduction to 2.78 %

The wattage of the resistor must be at least 7V X 1A X 2.78% = 0.195 W
So for this example a 1 watt resistor is suggested.

6.2 Armature pulse transformer circuit (Current driven)

This circuit is more common and much better.



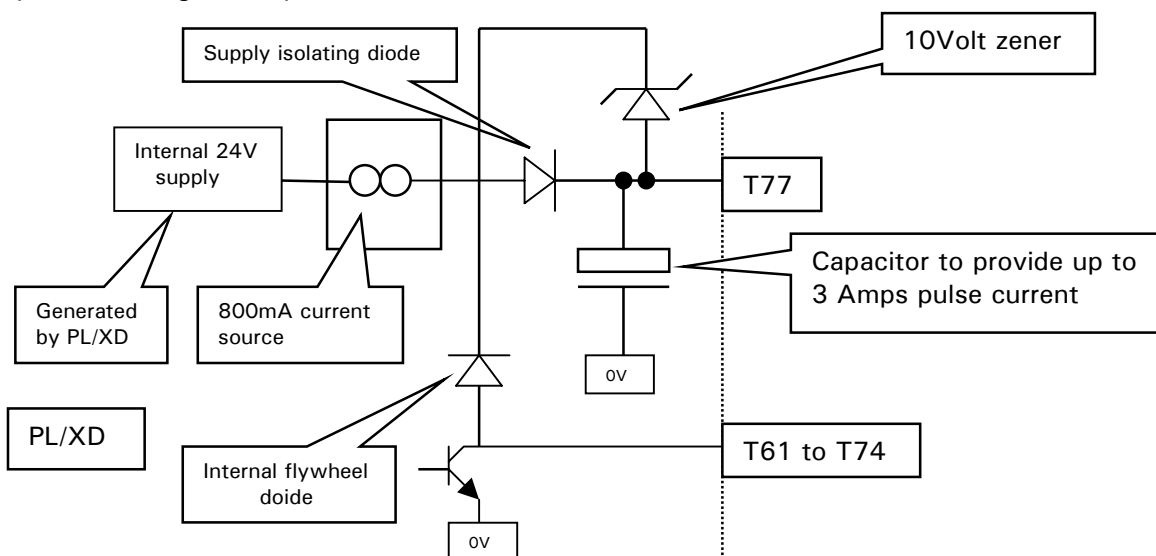
In this case the primary is current driven. This results in several advantages.

- 1) The pulse transformer Volts - seconds rating can be much lower because it only has to support the reflected gate voltage. This means the pulse transformer can be smaller.
- 2) If the transformer saturates there is no harm done because the primary current is limited by the resistor.
- 3) The transformer output will automatically keep rising until it reaches the required gate trigger voltage.

Example. The pulse transformer has a 2 : 1 ratio. The desired gate current is 1 amp.
 Assume the diode drop and gate voltage are 3 volts. Hence the reflected secondary voltage will 6V.
 Assume worst case primary voltage of 20V. Then $20 - 6 = 14V$ will be across the resistor
 For 1 amp gate current, the primary current must be 0.5A hence the resistor must be 28 Ohms.
 The resistor watts are $14V \times 0.5 \times 2.78\% = 0.195$ Watts. So for this example a 1 watt rating is suggested.

6.3 24V supply and internal flywheel diode

The supply is fed through a current source of 800mA capability. The current source charges the reservoir capacitor via an isolating diode. When the transistor turns on, the capacitor supplies the peak current of 1.5A. The capacitor is recharged during the off periods. When the transistor turns off, the pulse transformer will flywheel through the flywheel diode and zener.



In the event of a short circuit the current source will limit the steady state short circuit current to a maximum of 800mA.

The isolating diode allows an external supply to be added. See 6.4 Using an external 24V supply.

6.4 Using an external 24V supply

There are 6 outputs for the forward bridge and 6 for the reverse bridge. The internal supply is capable of providing a maximum of 1.5 Amps drive for each gate on each bridge.

When the parallel 2 quadrant mode of operation is selected it is possible to use the R outputs to drive a parallel 2Q stack. See 4.3 Armature bridge 2 quadrant parallel. If this is required the rating will be reduced to 0.75A per gate drive due to the limitations of the +24V power supply. This is because all 12 outputs will be working together. (Note. The Pulse transformer unit LA102800 requires 1.5A per channel hence may be operated in this mode for parallel 2Q stack configurations, provided that an external 24V supply is available to provide a further 800mA of current. See 13 Pulse transformer unit (LA102800))

The supply should be current limited so that a short circuit will not cause damage. The 0V of the supply should be connected to terminal 36 on the control card. The +24V of the external supply should be connected to terminal 77.

7 Internal or External field bridge option

The PL/XD has a built in field bridge that can supply up to 32 Amps field current. There is also a version that can supply up to 50 Amps model PL/XD50A. Provision has been made to allow an external field bridge to be controlled. This may be required if more Amps, or a higher AC supply must be accommodated.

7.1 Internal field bridge

The internal field bridge is supplied with AC power through terminals EF2 and EF3. **The supply must be in phase sequence with EL2 and EL3.**

The normal application for stacks up to 480V AC is to **link EL2 to EF2 and EL3 to EF3.**

Note. Ensure that semiconductor fuses are used in the AC supply to protect the field bridge. The maximum I²t for these fuses is 5000.

For AC supply voltages in excess of 480V AC and up to 690V AC it is necessary to interpose a single phase reduction transformer of sufficient rating between EL2/3 (rated up to 690V AC) and EF2/3 (rated up to 480V AC only) to maintain the internal field bridge supply within the 480V AC rating. The phase lag or lead across this transformer must be kept as low as possible to ensure correct firing of the internal bridge.

Note. The internal field bridge is rated to supply up to 32 Amps for model PL/XD, or 50 Amps for model PL/XD50A. By using the code switches it is possible to select 2 rating configurations. These are
 3,000 armature amps range, and 32 field amps range
 30,000 armature amps range, and 64 field amps range.

Whichever range is used the unit will automatically rescale the field current to give the full model field current at the limit of the field current range selected. See 9.2 679)ID ABCXRxxx MON.

- 1) If the 32 Amp range is selected on the standard 32 amp unit then the displayed current will be correct.
- 2) If the 64 Amp range is selected on the standard 32 amp unit then the displayed current will be actual x 2.

There is a special reserved menu setting that allows a 50Amp and a 100Amp scale on the display.

- 3) If the 32 Amp range is selected, then the display will extend to 50A if it is set in the reserved menu.
- 4) If the 64 Amp range is selected, then the display will extend to 100A if it is set in the reserved menu.

7.2 External field bridge

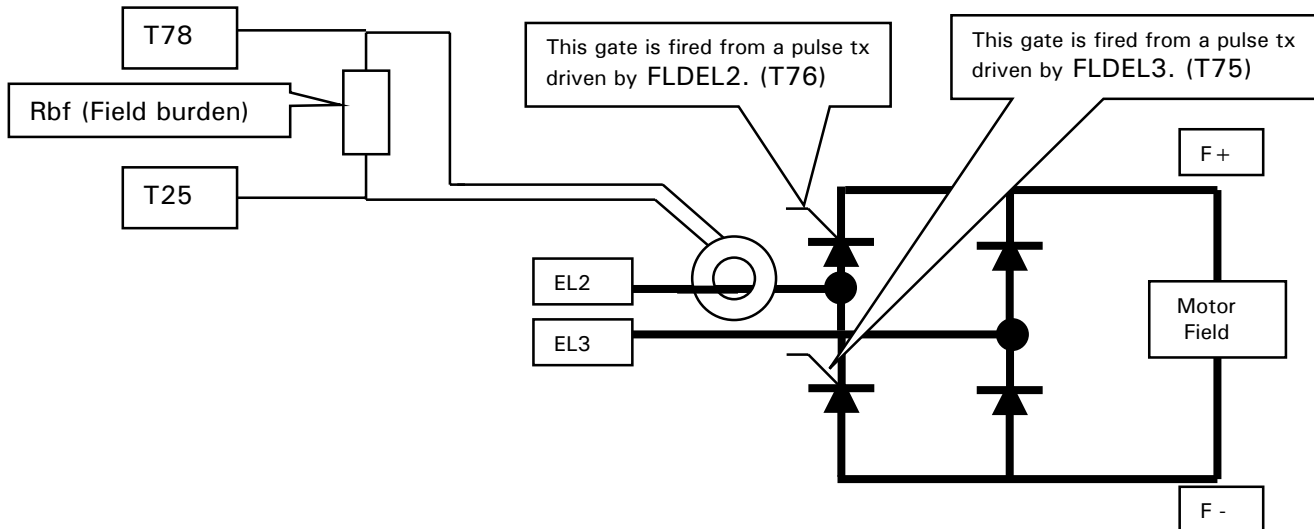
Gate pulse transformer primary drivers are provided to control an external field bridge. The external bridge must be supplied from an AC source that has the same phasing as EL2 and EL3.

When using an external field bridge, the internal field bridge terminals EF2/3 and F+ F- are left disconnected.

Note. It is possible to select a configuration that gives 30,000 armature amps range, and 64 field amps range. See 9.1 Procedure for changing stack code bridge configuration and current ranges.

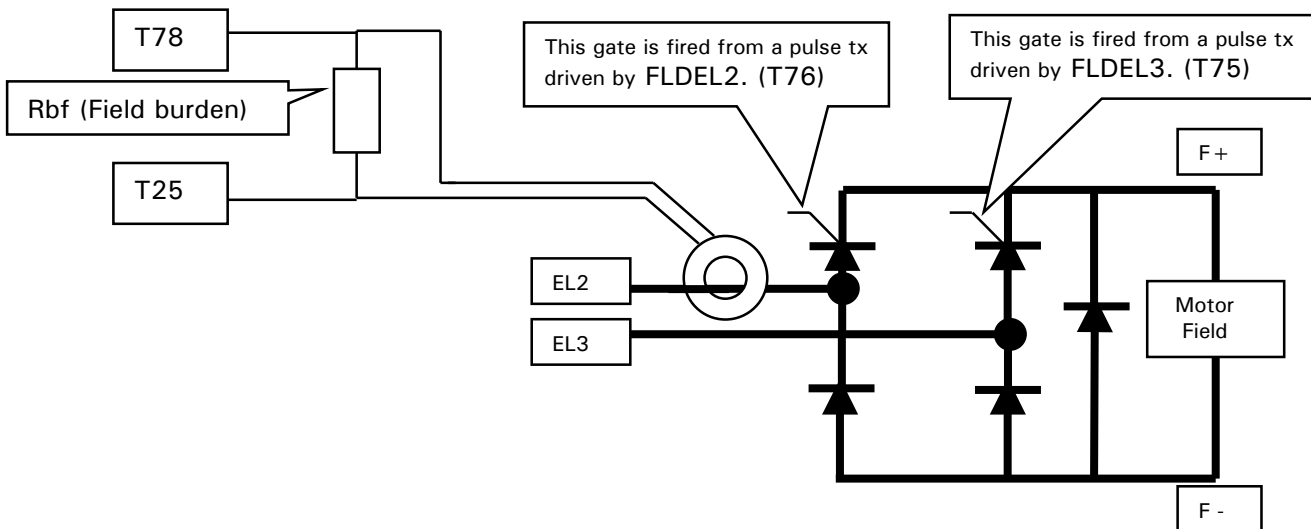
The field bridge must be half controlled with a flywheel diode. There are 2 common bridge configurations.

7.2.1 External field bridge with phase leg thyristors



The field current must be sensed by using a current transformer (Acct) on the AC supply to the field bridge. See 7.3 Calibrating an external Field Acct. See also 13 Pulse transformer unit (LA102800), which has provision for mounting Rbf.

7.2.2 External field bridge with separate flywheel diode



7.3 Calibrating an external Field Acct

The PL/XD may be set by the code switch to be either 32A or 64A max field range on the display. See 9.1 Procedure for changing stack code bridge configuration and current ranges, and 7 Internal or External field bridge. It may also be desired to provide fields in excess of the standard display ranges.

When using an external field bridge with a rating in the range 1- 32A it is preferable to code the PL/XD for the 32 Amp range. For fields between 32 - 64A it is preferable to code the PL/XD for the 64 Amp range. Maximums within these ranges can then be set on 4)RATED FIELD AMPS in the Calibration menu. For fields above 64A it is preferable to code the PL/XD for the 100 Amp range, by a setting in the reserved menu, (refer to supplier for assistance) however it will not be possible in this case, for the display to agree with the actual field current for currents above 100 Amps. However this limitation may be mitigated by calibrating the external field so that the display will show some convenient factor eg. half actual current.

For a 100 % output, (irrespective of the selected range) the external Field Acct must provide 1.512 Volts at terminal T78 referred to common at T25.

The input resistance to this terminal is 189 Ohms. Hence your field burden is in parallel with 189 Ohms.

This means that you must first calculate the maximum secondary current signal in the field Acct for the full range field current, (e.g usually 32 or 64 Amps) then calculate what external burden resistor you require which when placed in parallel with 189 Ohms gives a voltage of 1.512 Volts if the full range current was flowing. Having matched the burden for the full range then 4)RATED FIELD AMPS in the Calibration menu is used to provide precise calibration for the desired maximum and the displayed units will be correct.

Alternatively use the formula below for your selected range.

After this process when 32A or 64A (depending on selected range code) is flowing in your field, then the field display will indicate the correct current 32A or 64A (depending on selected range code).

Remember that the actual field current calibration is then set within the range by 4)RATED FIELD AMPS.

7.3.1 Formula for calculating external field burden (Rbf) for 32A maximum.

$$\text{External Rbf} = 189 / ((4000 / \text{turns}) - 1)$$

Divide the number of turns on the Field Acct into 4000. Then subtract 1. Divide the result into 189.

The answer is the external Field Acct burden resistor in Ohms. (Rbf)

Example. What is the field Acct burden resistor value for an Acct with 1000 turns?

$$4000 / 1000 = 4, \quad 4 - 1 = 3, \quad 189 / 3 = 63 \text{ Ohms.}$$

Note for 'turns' of 4000 the result is infinity hence no resistor is needed.

Fit a 63 Ohm resistor combination across the Field Acct. Connect one end to 0V Terminal 25 and the other end to Terminal 78.

7.3.2 Formula for calculating external field burden (Rbf) for 64A maximum.

$$\text{External Rbf} = 189 / ((8000 / \text{turns}) - 1)$$

Note for 'turns' of 8000 the result is infinity hence no resistor is needed.

7.3.3 Formula for calculating external field burden (Rbf) for currents from 64A to 128A

$$\text{External Rbf} = 189 / ((16000 / \text{turns}) - 1)$$

In this case when 128Amps is flowing it will only display 64A on the display for 100% current, and hence 4)RATED FIELD AMPS must be set to half your desired field current. Eg for 100 Amps set it to 50Amps.

7.3.4 Orientation of the external Field Acct

It is important to have the correct polarity of field current feedback from the external field Acct.

The feedback circuit will work irrespective of the polarity, however the accuracy will be compromised if the polarity is wrong.

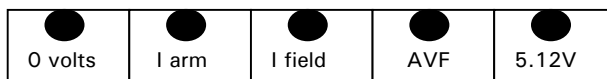
Factors that influence the polarity are:

- 1) Direction of windings on the Acct.
- 2) Orientation of Acct on primary cable.
- 3) Choice of primary cable. (EL2 or EL3).

A signal pin is provided to enable the polarity to be checked.

7.3.5 Signal test pins

There is a row of test pins just behind the middle control terminal used to monitor certain feedback signals.



The I field signal may be used to observe the field feedback signal superimposed on the EL2 / EL3 AC sine wave. Display this signal on an oscilloscope. Before exciting the field reduce FIELD CONTROL / 100)FIELD VOLTS OP % to 0.00%. This will allow you to gradually increase the field phase angle whilst observing the signal on the test pin, and at the same time ensuring that the actual field current is scaled as expected.

Before doing this test you must be satisfied that the installation is safe and ready to receive power to the motor.

You must have selected the correct stack code for your application. See 9.1 Procedure for changing stack code bridge configuration and current ranges. See also 9.2 679)ID ABCXRxxx MON.
Set 4)RATED FIELD AMPS to a suitable value to suit the motor field.
Set 100)FIELD VOLTS OP % to 0.00%.
Set 111)STANDBY FLD ENBL to DISABLED.
Set 112) STANDBY FLD CUR to 100.00%.

Prepare to observe the signal on the I Field test pin. Apply EL1 / EL2 / EL3 AC auxiliary supply.
Observe supply is correct on 169)EL1/2/3 RMS MON

Set 111)STANDBY FLD ENBL to ENABLED.

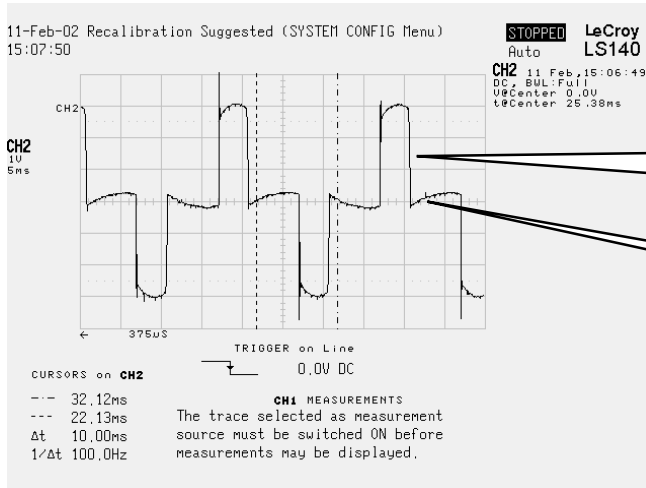
Carefully increase 100)FIELD VOLTS OP % whilst observing the signal on the I Field test pin. During this operation you should see the field current feedback signal appearing superimposed on the EL2 / 3 waveform. It will advance in phase angle and increase in amplitude as you increment 100)FIELD VOLTS OP %. During this process you should also check that the field current is under control and of the expected magnitude.

Now you can observe the polarity of the signal.

If the polarity is incorrect then it can be changed by transposing the connections from the Field Acct. Repeat the test after transposing the wires and then check the accuracy of the feedback by monitoring 145)FLD CUR AMPS MON. Note. Very low currents (< 5%) may not be accurate.

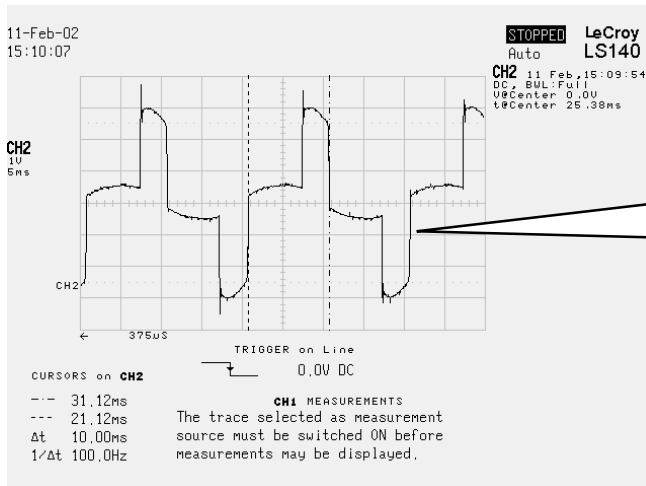
When the test is finished restore 100)FIELD VOLTS OP %, 111)STANDBY FLD ENBL, 112) STANDBY FLD CUR to the required system settings.

7.3.5.1 Oscilloscope traces of the I Field signal



This is the **correct polarity**. The current signal moves in the opposite direction to the EL2 / EL3 signal

This is the EL2 / EL3 signal



This is **incorrect**. The current signal moves in the same direction as the EL2 / EL3 signal. In this case swap the Field Acct connections and recheck.

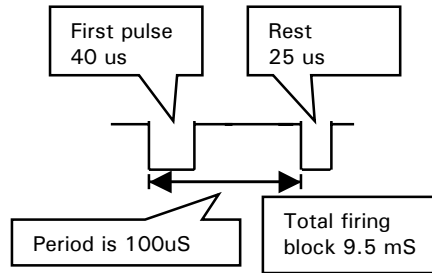
7.4 External field thyristor gate waveform

All pulse transformers must have an isolation voltage of at least 4 times AC volts plus 1000V.

Eg for 480 volts AC, isolation voltage rating must be at least 2920 Volts.

Also the interwinding capacitance must be as low as possible and not in excess of 10 picofarad.

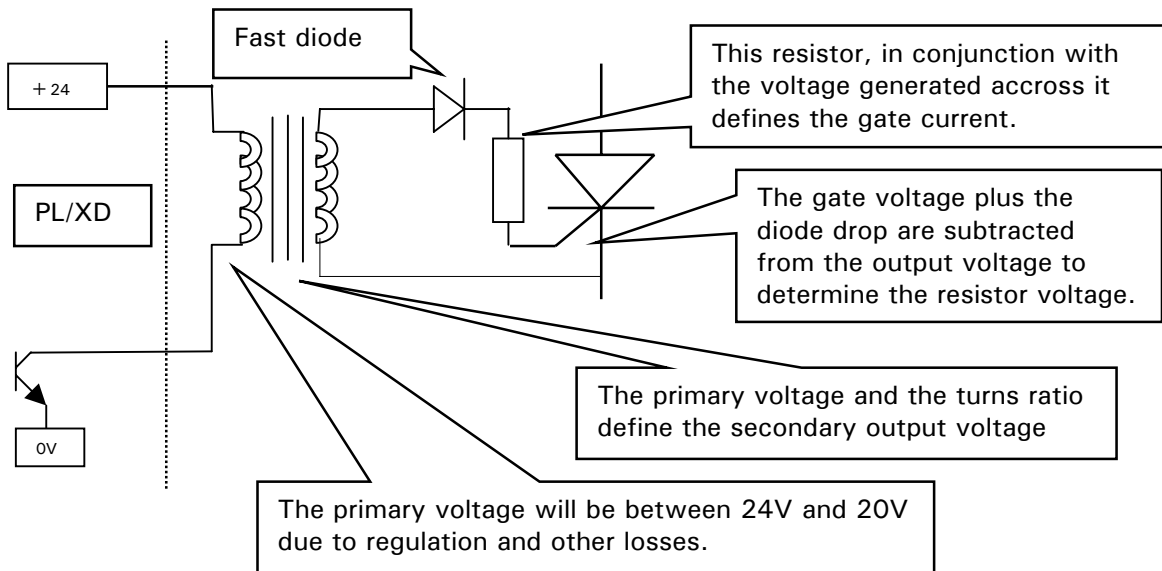
The firing pulse for the thyristor on EL2 is on terminal 76 (FLDEL2) and for EL3 is on terminal 75 (FLDEL3). (Do not confuse with EF2 and EF3 unused internal field connections). The pulse outputs are open collector. The maximum current sinking capability of each output is 0.4 Amps. DO NOT EXCEED this current.



7.4.1 Field pulse transformer circuit (Voltage driven)

This circuit is quite common but the current drive method discussed in the next section is much better. (The diagram below is a simplistic circuit, there may be other components e.g. gate shorting resistors).

This type of circuit requires a pulse transformer that can support the drive voltage for at least 40 uS (Volt-seconds). In practice there would need to be a large margin of safety to take account of primary voltage and pulse timing tolerances. If the pulse transformer were to saturate due to an insufficient Volt-seconds rating then the primary circuit would be short circuited.



Example. The pulse transformer has a 2 : 1 ratio. The desired gate firing current is 0.32 amp.

Assume worst case primary voltage of 20V. Hence output secondary voltage will be 10V.

The voltage across the resistor will be $(10 - \text{diode drop} - \text{gate voltage}) = 7V$

Hence for 0.32 amp gate current the resistor must be 22 Ohms. (The primary current will be 0.16A).

The average primary current will be reduced by duty cycle. 25% (waveform) $\times 47.5\%$ (thyristor) = 12%

Note the dissipated watts will be $7V \times .32A \times 12\%$ duty cycle = $0.27W$. So use at least a 1 watt resistor.

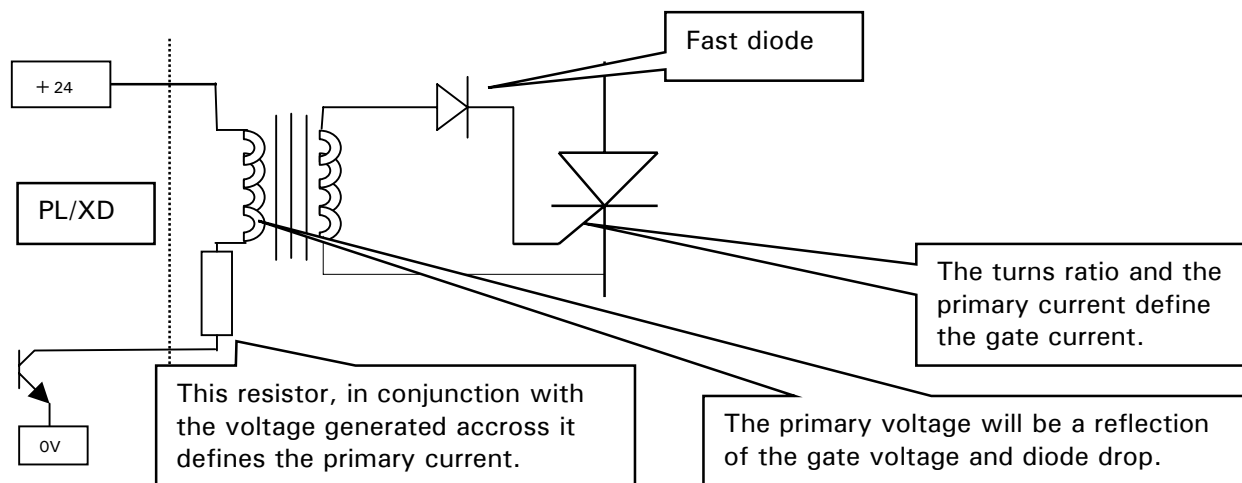
7.4.2 Field pulse transformer circuit (Current driven)

All pulse transformers must have an isolation voltage of at least 4 times AC volts plus 1000V.

Eg for 480 volts AC, isolation voltage rating must be at least 2920 Volts.

Also the interwinding capacitance must be as low as possible and not in excess of 10 picofarad.

This circuit is more common and much better.



In this case the primary is current driven. This results in several advantages.

- 1) The pulse transformer Volts - seconds rating can be much lower because it only has to support the reflected gate voltage. This means the pulse transformer can be smaller.
- 2) If the transformer saturates there is no harm done because the primary current is limited by the resistor.
- 3) The transformer output will automatically keep rising until it reaches the required gate trigger voltage.

Example. The pulse transformer has a 2 : 1 ratio. The desired gate current is 0.32 amp.

Assume the diode drop and gate voltage are 3 volts. Hence the reflected secondary voltage will 6V.

Assume worst case primary voltage of 20V. Then $20 - 6 = 14V$ will be across the resistor

For 0.32 amp gate current, the primary current must be 0.16A hence the resistor must be 87.5 Ohms.

The average primary current will be reduced by duty cycle. 25% (waveform) \times 47.5% (thyristor) = 12%

Note the dissipated watts will be $14V \times .16A \times 12\%$ duty cycle = $0.27W$. So use at least a 1 watt resistor.

8 Armature voltage feedback

The max armature voltage possible is +/- 1000V. Plug in screw terminals are provided for the Armature voltage. Higher voltages may be prescaled prior to connection to the PL/XD.

Connect the A+ to terminal T41
 Connect the A- to terminal T43

Note. The monitor in DIAGNOSTICS / 126)ARM VOLTS MON is clamped at 1.25 times the setting of CALIBRATION / 18)RATED ARM VOLTS

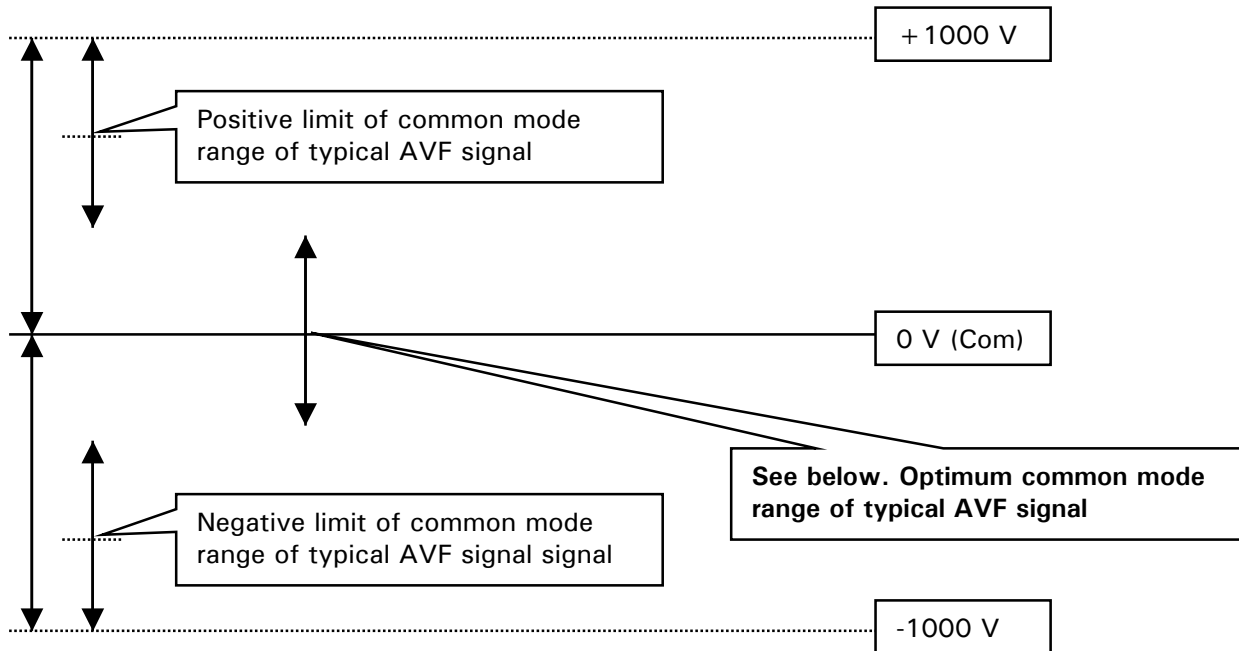
8.1 Common Mode Range

The maximum input voltage of T41 or T43 is +/-1000V with respect to 0 Volts. (Common).

Hence an AVF signal of 1000 volts may at the limit have one side at the same voltage with respect to 0 Volts (Common) and still measure linearly.

An AVF signal of 500 volts may have one terminal at + 500 V with respect to 0 Volts (Common) and the other terminal at +1000V and still measure linearly.

The optimum common mode is for the +/- AVF signal to swing symmetrically with respect to 0 Volts (Common).



These are absolute limits. You should always make allowances for overshoots, ripple etc.

You should always try to ensure the armature voltage common mode range is as per the optimum if possible. If the neutral of the 3 phase supply is close to the earth (which is close to 0V common) then the common mode range will be optimum.

9 CONFIGURATION / DRIVE PERSONALITY

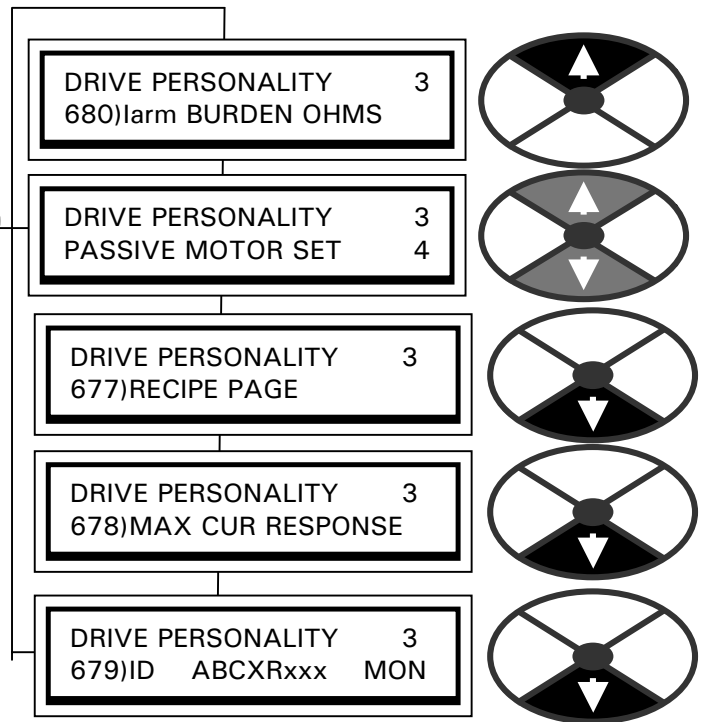
PIN numbers used 677 to 680
 This menu is used to modify or monitor various aspects of the PL/XD personality.



1) ID ABCXRxxx MON, is used to identify the power chassis and is not intended to be used for any other purpose. A binary code is displayed.

This code must be altered depending an armature current range, field current range and stack configuration.

2) Iarm BURDEN OHMS is used to alter the model maximum armature current, and allow the PL/XD diagnostics and settings to show the correct level of Amps according to the hardware burden resistor employed in the current feedback network. See How to calibrate the PL/XD armature current.



You must select the correct stack code for your application

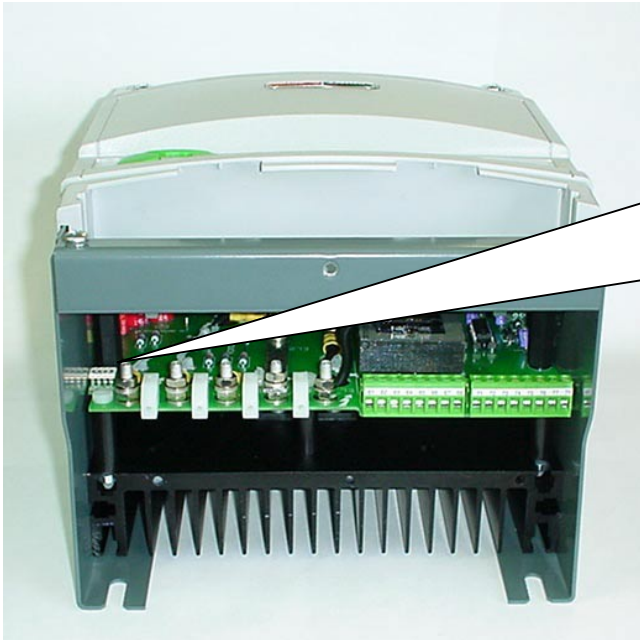
9.1 Procedure for changing stack code bridge configuration and current ranges

- 1) Turn off the unit completely.
- 2) Determine desired code for application. See next section.
 (Bridge configuration and current range for armature and field).
- 3) Set the switches accordingly. See next section.
- 4) Turn on control supply.
- 5) Check the new code has been recognised.
 CONFIGURATION / DRIVE PERSONALITY / 679)ID ABCXRxxx MON.

9.2 679)ID ABCXRxxx MON

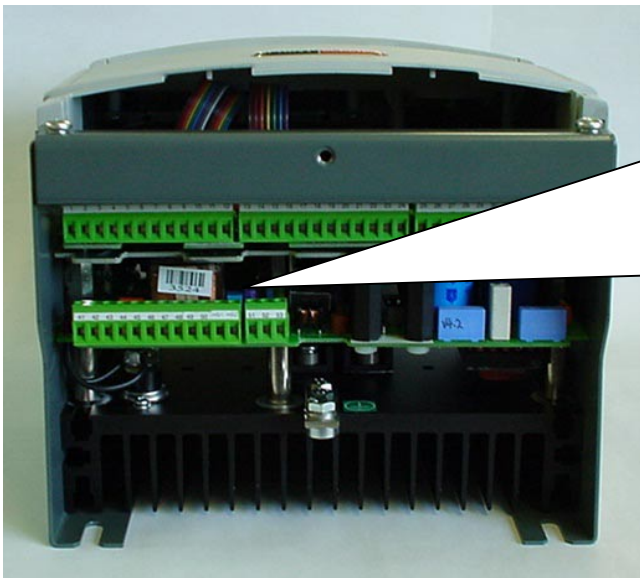
There are 2 sets of DIL switches on the power board

a) 4 way switch, and b) 2 way switch



a) 4 way switch (A B C R)
 1 = A ON = 0, OFF = 1
 2 = B ON = 0, OFF = 1
 3 = C ON = 0, OFF = 1
 4 = R ON = 0, OFF = 1

Switch up towards board edge to turn the switches ON.
 Please see the codes below for switches 1-4.



b) 2 way switch X (pole 2), FIRING (pole 1)
 2) = X ON = 0, OFF = 1 (back)
 1) = FIRING ON = 0, OFF = 1 (front)

The 2 way switch is located behind Term HS2
 1) FIRING at the front 2) X at the back.

Switch to the left to turn the switches ON.

When ON the switch 1) FIRING will inhibit the 24V firing pulse supply.

Please see the codes below for switch 2) X.

The code displayed for a 4 quadrant PL/XD unit. Drives a 12 thyristor anti parallel bridge.

679)ID	ABCXRxxx	MON	(note ABC R are on 4 way switch, X is on 2 way switch)
	10111000	Max Displayed Armature current	3000.0 Amps. Max Displayed Field 32 Amps.
679)ID	ABCXRxxx	MON	
	00111000	Max Displayed Armature current	30,000 Amps. Max Displayed Field 64 Amps.

The code displayed for a 2 quadrant PL/XD unit. Drives a single 6 thyristor bridge, or 2 bridges in parallel.

679)ID	ABCXRxxx	MON
	10100000	Max Displayed Armature current 3000.0 Amps. Max Displayed Field 32 Amps.
679)ID	ABCXRxxx	MON
	00100000	Max Displayed Armature current 30,000 Amps. Max Displayed Field 64 Amps.

To alter code. See 9.1 Procedure for changing stack code bridge configuration and current ranges.

Note. The physical limit of the application is a function of the external stack engineering not the unit displays.

9.3 How to calibrate the PL/XD armature current

This section describes how to calibrate the PL/XD and the external hardware burden resistor to give the desired armature current

9.3.1 Overview

There is the **HARDWARE BURDEN RESISTOR** supplied by the user, that must have a value calculated to provide a maximum -2V signal from the secondary Acct current. The -2V level represents the upper limit of adjustment for the PL/XD. For best calibration this upper limit will be at or slightly above the desired 100% motor current.

There is a **SOFTWARE BURDEN VALUE** (680)Iarm BURDEN OHMS) entered by the user into the PL/XD. This determines the range of adjustment in Amps for the calibration parameter 2)RATED ARMATURE AMPS.

The HARDWARE and SOFTWARE burden values are only the same value for Accts of 2000 turns. See 5 Armature Accts. For other turns ratios they will differ. See 9.3.4 Armature current Acct turns examples.

Procedure overview for calibration.

Step 1 Select the desired armature current range for the PL/XD and alter the code switches accordingly. There are 2 ranges (3000.0 or 30,000 Amps). See 9.2 679)ID ABCXRxxx MON for armature current range selection.

Step 2 Calculate software burden value for upper limit of armature current range and enter into PL/XD. CONFIGURATION / DRIVE PERSONALITY / 680)Iarm BURDEN OHMS. Then enter precise value of 2)RATED ARMATURE AMPS required.

Step 3 Calculate hardware burden to give -2V for current equal to upper limit. Select burden resistor combination to give required Ohms and wattage and install.

The following sections will describe the above steps.

9.3.2 Step 2. Calculate software burden value

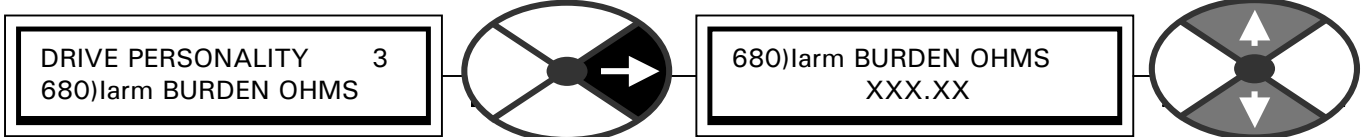
Use the following formula to calculate the desired **ideal** software burden value.

$$\text{Ideal software burden value (Ohms)} = 4000 / \text{Max armature current (Amps)} \quad \text{equation 1}$$

Higher values of the maximum current range require lower values of 680)Iarm BURDEN OHMS. The resolution becomes more coarse as you approach low values of 680)Iarm BURDEN OHMS because you can only enter its value to 2 decimal places.

E.g. 2,510 Amps motor rating ideally requires a burden of 1.594. However because you can only enter to 2 decimal places you have a choice of 1.60 or 1.59. This means that you can choose an upper limit of 1.60 = 2500A or 1.59 = 2,516 Amps. From equation 1. You must always choose an upper limit that includes your desired maximum so in this case you must enter 1.59 to give an upper limit of 2,516 Amps. Don't worry that this is higher than desired because final precise calibration occurs using the calibration menu parameter **2)RATED ARMATURE AMPS**.

Now you must enter the chosen value of software burden into the PL/XD. In the above example this is 1.59 giving an upper limit of 2,516 Amps.



This value is used to set the max PL/XD armature amps.	PARAMETER	RANGE	DEFAULT	PIN
	Iarm BURDEN OHMS	0.00 to 320.00	9.30	680

Note. After 680)Iarm BURDEN OHMS has been altered, it will only apply after the following steps:-

- 1) Save the new value using the PARAMETER SAVE function.
- 2) Turn the unit control supply off then back on again.
- 3) Adjust- 2)RATED ARM AMPS parameter in the CALIBRATION menu, first to its maximum setting (100%), and then to its minimum setting (33%), (Note values are 100% Amps, 33% Amps, of new range with changed software burden).
- 4) Take note of the upper limit of 2)RATED ARMATURE AMPS because you will use this to calculate the hardware burden value in due course.
- 5) Finally return 2)RATED ARM AMPS to the desired value for your motor.
- 6) Save the new desired 2)RATED ARM AMPS parameter with another PARAMETER SAVE.

So to use the above example to illustrate the above steps.

Desired motor 100% current is 2,510 amps.

Nearest upper limit of PL/XD range which includes desired rating is 2,516 Amps using value of 1.59 for 680)Iarm BURDEN OHMS.

Enter 1.59 and follow above procedure to permanently retain it.

In step 4, note upper limit of 2)RATED ARM AMPS is 2,516 Amps.

Take note of upper limit for calculation of hardware resistor.

Set 2)RATED ARM AMPS to 2,510.0 Amps and save.

9.3.3 Step 3. Calculate hardware burden

(The Accts will have, typically, between 500 and 10,000 turns each. All 3 Accts must have the same spec.)

The formula for calculating the hardware burden resistor value is as follows

Value in Ohms = $2V \times \text{Number of Acct turns} / \text{upper limit of 2)RATED ARMATURE AMPS}$. Equation 2

Following the above example

For 2510 amps armature current rating the PL/XD has been calibrated to give an upper limit of 2516A. With a software burden of 1.59.

Hence the correct procedure is to calculate the hardware burden to match the upper limit of the PL/XD ie. 2516A.

Using the formula for Accts with 2000 turns.

Value in Ohms = $2V \times 2000 / 2516 = 1.59 \text{ Ohms}$. (notice that for 2000 turns the hardware and software values are the same)

Hence in this example we must fit a hardware burden resistor of 1.59 Ohms.

See 9.3.4 Armature current Acct turns examples, to see the effect of calculating for Accts with more or less than 2000 turns.

9.3.3.1 Calculating required wattage

Using previous example

The armature current can range up to 2516A and this is divided by the number of turns to give the secondary burden current.

Secondary burden current = 2516 Amps / 2000 Acct turns = 1.258A.

The wattage of the burden resistor must be rated for 150% current to accommodate PL/XD overload capability = 1.258 X 1.5 = 1.887 Amps

So wattage = I squared R = 1.887 x 1.887 x 1.59 = 5.66 Watts.

In this case a 10 Watt Burden resistor rating would be recommended to prevent excessive heating effect in the resistor. As a rule of thumb the total wattage of the hardware burden resistor (Rb) combination must be approximately 20 / Rb.

9.3.3.2 Optimum resistor combination

In the example the resistor required is 1.59 Ohms at 10 Watts.

A good strategy is to use 2 higher value resistors in parallel to provide a value slightly above the desired target and provide the wattage requirement, then a third much larger value in parallel to trim it down.

Hence choose two 5 watt resistors of 3.3 OHMS in parallel to give $3.3 / 2 = 1.65$ Ohms.

Then calculate the third parallel resistor to trim it to 1.59

$$1 / 1.59 = 1 / 1.65 + 1 / R$$

Third resistor = 44 Ohms.

Note. Because this resistor is a much higher value than the other 2, its accuracy has only a small effect on the overall combination accuracy.

9.3.4 Armature current Acct turns examples

Simple examples showing calculations for Accts of 4000 and 1000 turns

Note the **software** burden calculation does not depend on the actual Acct turns.

Hardware Burden

Value in Ohms = 2V X Number of Acct turns / upper limit of 2)RATED ARMATURE AMPS.

Example 1) Accts of 3000 turns. Motor rating of 25,000 amps max.

Software burden 680)Iarm BURDEN OHMS = 0.16

In this case the actual hardware resistor for 25,000 amps will be higher at 0.24 Ohms because there are more than 2000 turns and more turns means less signal current.

(Signal current across burden resistor must make -2V at upper limit of PL/XD).

Example 2) Accts of 1000 turns. Motor rating of 8000.0 amps max.

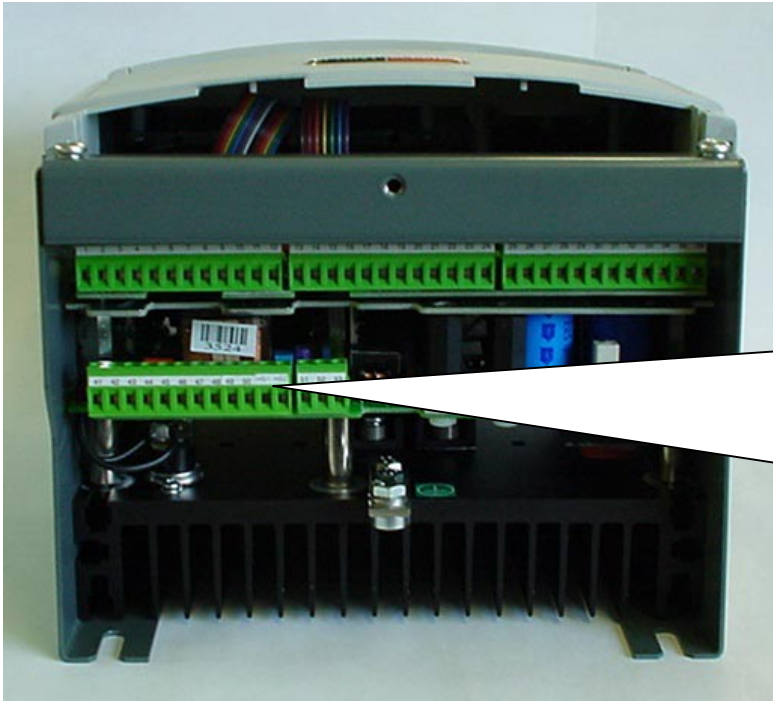
Software burden 680)Iarm BURDEN OHMS = 0.50

In this case the actual hardware resistor for 8000.0 amps will be lower at 0.25 Ohms because there are less than 2000 turns and less turns means more signal current.

(Signal current across burden resistor must make -2V at upper limit of PL/XD)

The above conveniently precise examples have been chosen to illustrate the effect of different Acct turns

10 External heatsink sensor.



External volt free overtemp switch connected to terminals HS1, HS2.

Note. This contact is in series with the unit heatsink sensor, so the alarm will activate for either the main stack heatsink, or the unit heatsink.

The alarm activates when the switch is open.

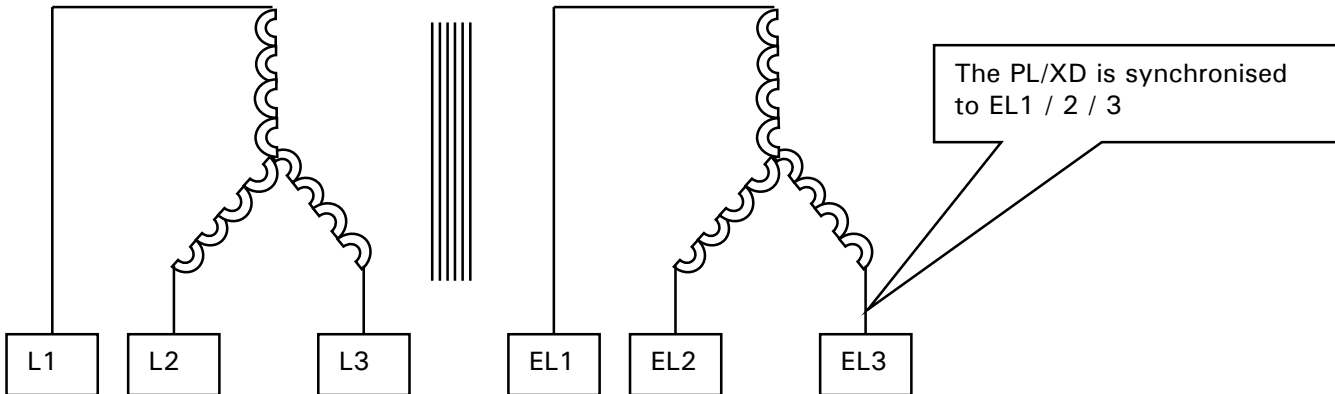
These terminals must be shorted together if there is no external temperature switch.

11 Synchronisation to the AC supply

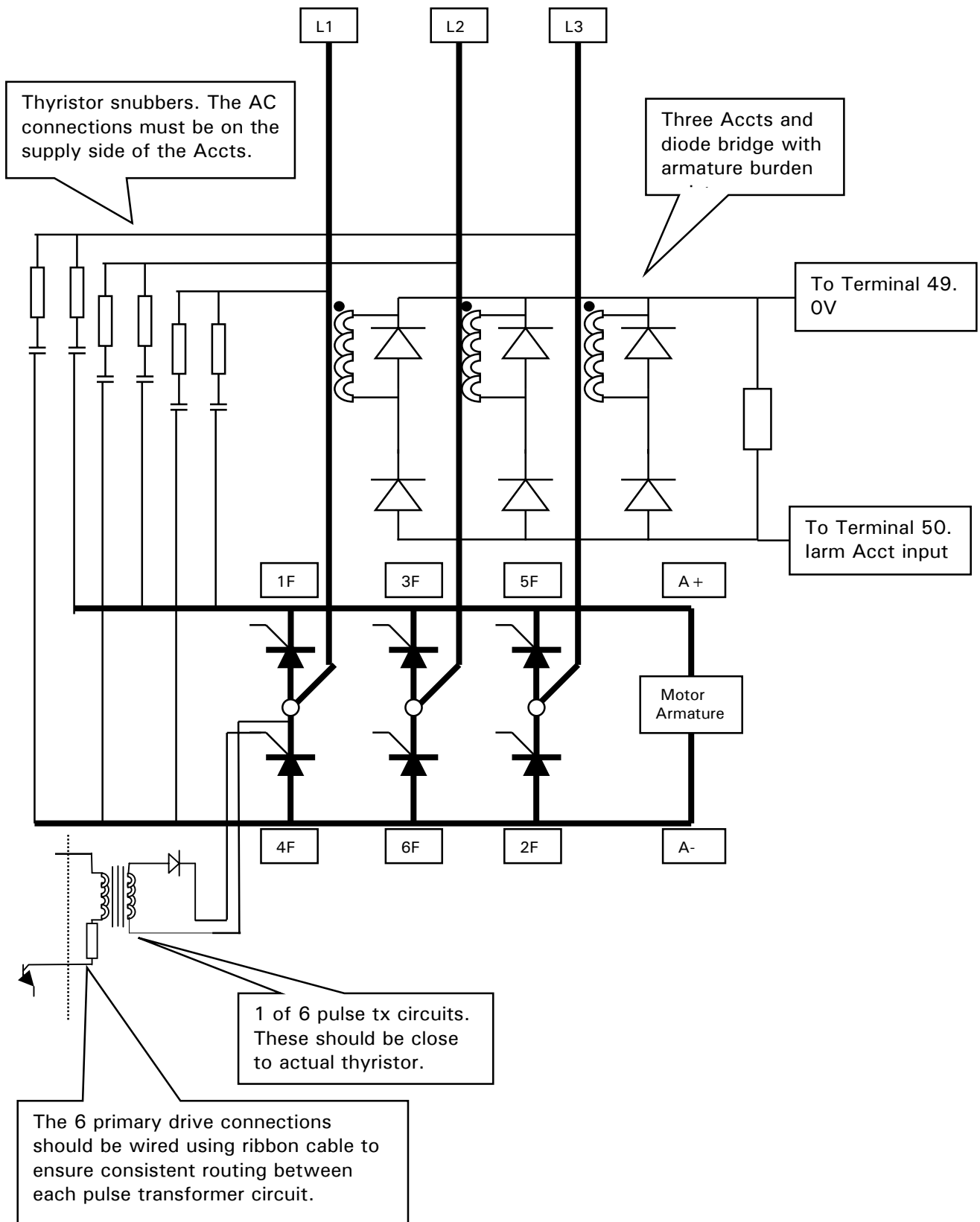
Synchronisation to the AC supply is achieved by monitoring EL1 / 2 / 3. Hence if for whatever reason it is necessary to insert a transformer between the L1 / 2 / 3 connections and the EL1 / 2 / 3 or EF2 / 3 connections then it is essential that the phase relationship between the sets of terminals is maintained.

There may unfortunately be a few degrees of lag or lead between caused by an external transformer. In this case it will be necessary to compensate for this by adjusting a parameter in a special menu reserved for factory use only.

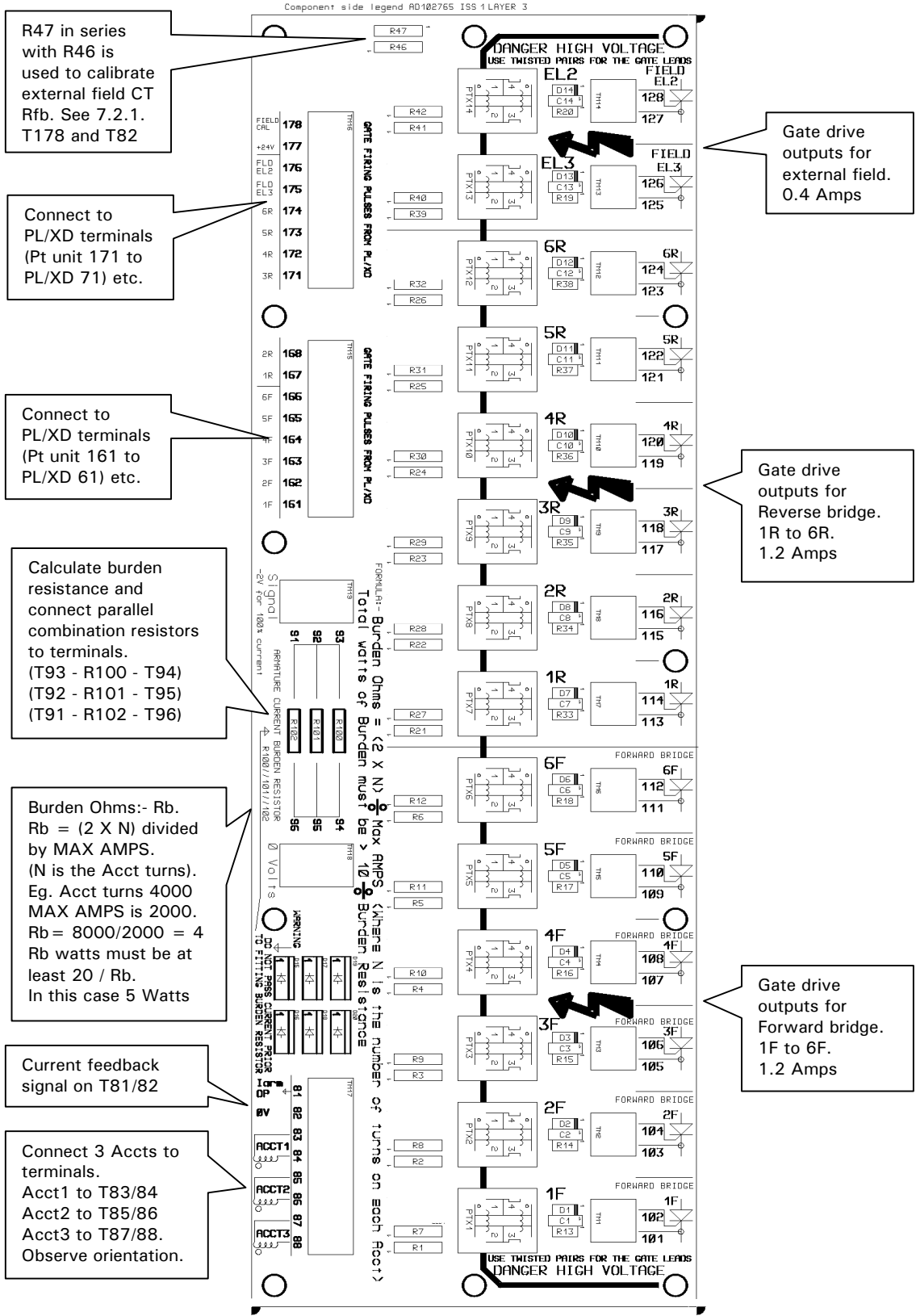
A typical example is a step down transformer from L1 / 2 / 3 to EL1 / 2 / 3.



12 Armature stack, snubbers, Accts and pulse tx circuit diagram



13 Pulse transformer unit (LA102800)

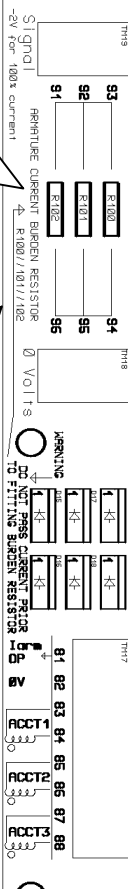


Component side Legend AD102765 ISS 1 LAYER 3

DANGER HIGH VOLTAGE
USE TWISTED PAIRS FOR THE GATE LEADS

USE TWISTED PAIRS FOR THE GATE LEADS
DANGER HIGH VOLTAGE

Formula:- Burden Ohms = $(2 \times N) \div \text{Max AMPS}$ (where N is the number of turns on each Acct)
Total Watts of Burden must be $> 10 \div \text{Burden Resistance}$



The Pulse transformer unit (Pt unit) is available at extra cost for users who do not wish to use their own systems.

It contains all the external interface components required to combine the PL/XD with the thyristor stack and its associated Accts.

12 pulse transformer networks for 2 or 4 quadrant bridges. Gate drive current 1.2A rise time < 1 uS.

Breakdown Isolation voltage 3Kv

2 pulse transformer networks for an external field bridge. Gate drive current 0.4 A rise time < 1 uS.

Breakdown Isolation voltage 3Kv

An armature burden rectifier network. Max burden current 5 Amps.

Screw terminals for user burden resistors.

Screw terminals for 3 user Accts.

Screw terminals for connection to PL/XD via ribbon cable.

2 way screw terminals for each thyristor gate.

The unit is designed to be mounted on a DIN rail

The Pulse transformer unit card dimensions are 305mm by 107 mm. The card is mounted in a standard DIN rail mounting carrier assembly with overall dimensions of 325mm by 112mm, with 2 DIN rail clips.

13.1 Wiring instructions

Terminals 61 to 78 on the PL/XD are wired one to one to terminals 161 to 178 on the Pt unit.

It is recommended that these connections are made using a ribbon cable or independant loom to ensure that there are no loops which may cause false triggering due to the fast nature of the current pulses.

The armature Accts must each have the same orientation on L1, L2, L3 and also the thyristor snubbers **must have their AC supply connections on the supply side of the Accts**. This prevents erroneous current readings from the snubber current edges. **The field bridge supply must also be taken from the supply side of the Accts.**

The thyristor gate connections must be kept as short as possible and each gate must be wired with its own individual twisted pair. Please ensure that if necessary the gate wires are protected from hot components eg busbars etc.

See 13 Pulse transformer unit (LA102800) for further notes.

14 Record of Stack Driver manual modifications

Manual Version	Description of change	Reason for change	Paragraph reference	Date	Software version
5.01	First publication of Stack Driver Manual			Feb 2002	5.01
5.02	Internal field bridge supply terminals separated from EL1/2/3 synch terminals. New field bridge supply terminals called EF2 and EF3.	Allows more flexibility with stack voltages higher than 480V AC because EL1/2/3 are rated up to 690V AC		April 2002	5.01
5.11	Description of Pulse transformer unit added	Introduction of Pulse transformer unit	13	Sept 2002	NA
5.12	No changes to stack driver manual. See main manual for changes to general functionality	Functionality improvements	Main manual	Jan 03	5.12
5.13	Changed part number for pulse TX board Improve description of calibration procedure Code switch for C now set to a 1 to activate dynamic diagnostics.		13 9.2	July 2003 Oct 2003	5.12
5.14	Improve description of external field burden calculation	Description incorrect for 64A range	7.3	April 2004	5.12
5.15	Introduce PL/XD50A for 50 Amp internal field rating Modifications to Pulse transformer board description	Extra field current option become available Minor spec changes to PTX board	7.2 13	June 2007	5.15
5.15b	Introduce PL/XD50A for 50A and 100 Amp field scale selection in reserved menu. Consult supplier.	Improvement	7.1	Aug 2007	5.17
5.15h	Add details of slip ring motor applications	New proven application	4.4	Mar 2011	5.21

15 Record of Stack Driver bug fixes

Manual Version	Description of change	Reason for change	Paragraph reference	Date	Software version
5.01	First issue of Stack Driver			Feb 2002	5.01
5.02	No bugs recorded.			April 2002	5.02
5.11	No bugs recorded.			Sept 2002	NA
5.12	No bugs recorded			Jan 2003	5.12
5.13	No bugs recorded			Oct 2003	5.12
5.14	No bugs recorded			April 2004	5.12
5.15	No bugs recorded			June 2007	5.15
5.15	Field current loop becomes in-operative for 4)RATED FIELD AMPS set above 31.25% of max rating. Bug fixed for software version 5.17 and above.	Work round. For field currents above 31.25% of model rating use 100)FIELD VOLTS OP % to set field current to the correct level. For field weakening applications Upgrade software.	6.1.4 6.9.3	Oct 08	5.15
5.15	Field current loop becomes in-operative for 4)RATED FIELD AMPS set above 31.25% of max rating. Bug fixed for software version 5.17 and above.	Bug fixed	6.1.4 6.9.3	Oct 08	5.17

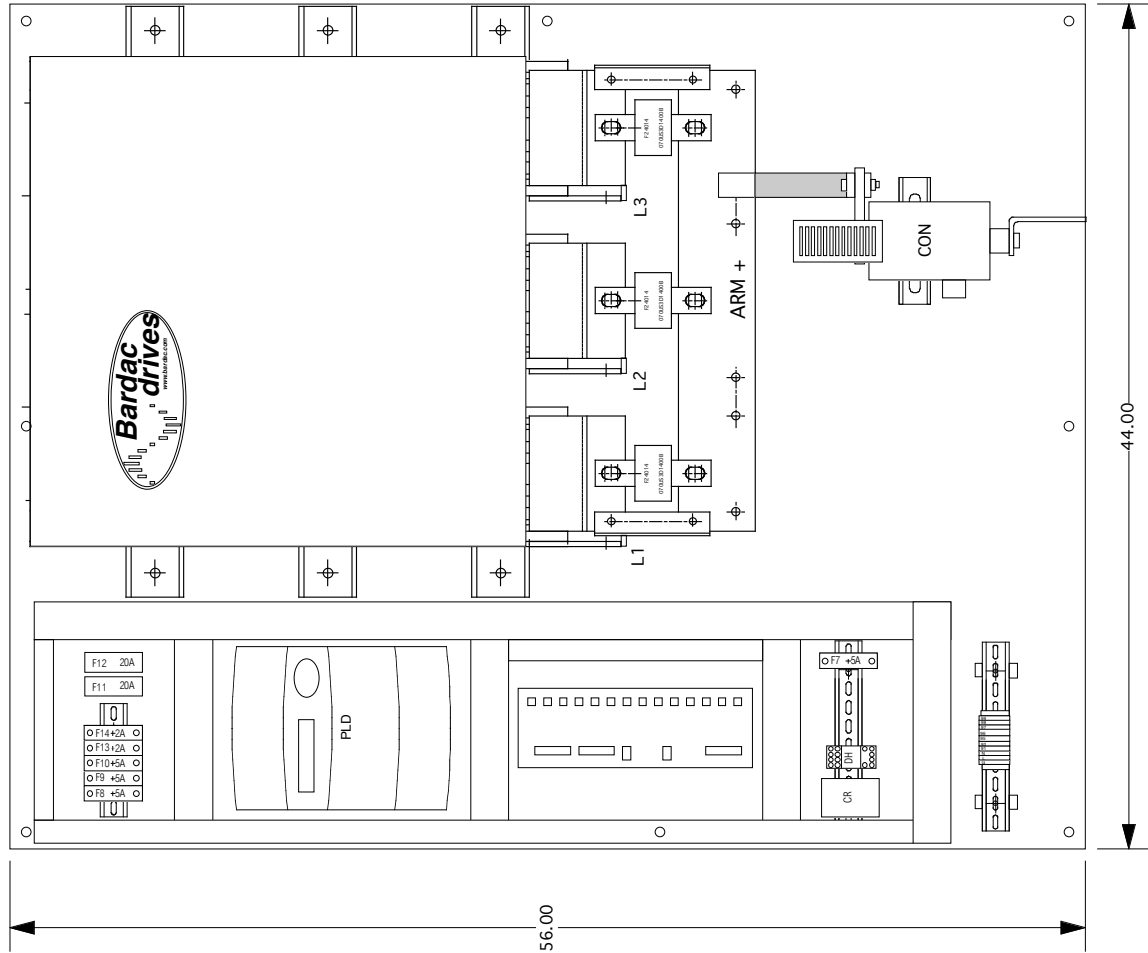
This record only applies to the Stack Driver . Please refer also to the product manuals for other bug fixes.

16 Changes to product since manual publication

Any new features that affect the existing functioning of the unit, that have occurred since the publication of the manual, will be recorded here.

1 2 3 4

A B C D



DRIVE PANEL TO MOUNTED TO BACK PANEL. ENSURE WHEN MOUNTING THERE IS SUFFICIENT CLEARANCE FOR MOTOR AND SUPPLY CABLES AT THE BOTTOM OF ENCLOSURE. A MINIMUM OF 8 INCHES SHOULD BE LEFT AT TOP OF PANEL TO ALLOW STACK FANS TO PROPERLY VENT.

ISS	DATE	APPROVED

SHT. TITLE	EXTERNAL STACK PANEL OUTLINE	CUST.	ANY CUSTOMER	DRN.	ENGINEER	DWG. NO.	HJ
DWG. TYPE	PANEL ASSEMBLY DIAGRAM	DIST.		DESIGN	ENGINEER	DWG. ISS.	PRE
JOB TITLE	950A DRIVE PANEL	P.O.		SCALE	10:1	JOB NO.	N/A
LOCATION				SIZE	A	SHT.	1 OF 1
				3			4

Bardac
 40 Log Canoe Circle, Stevensville, MD 21666
 phone (410) 604-3400, fax (410) 604-3500
 email: info@bardac.com

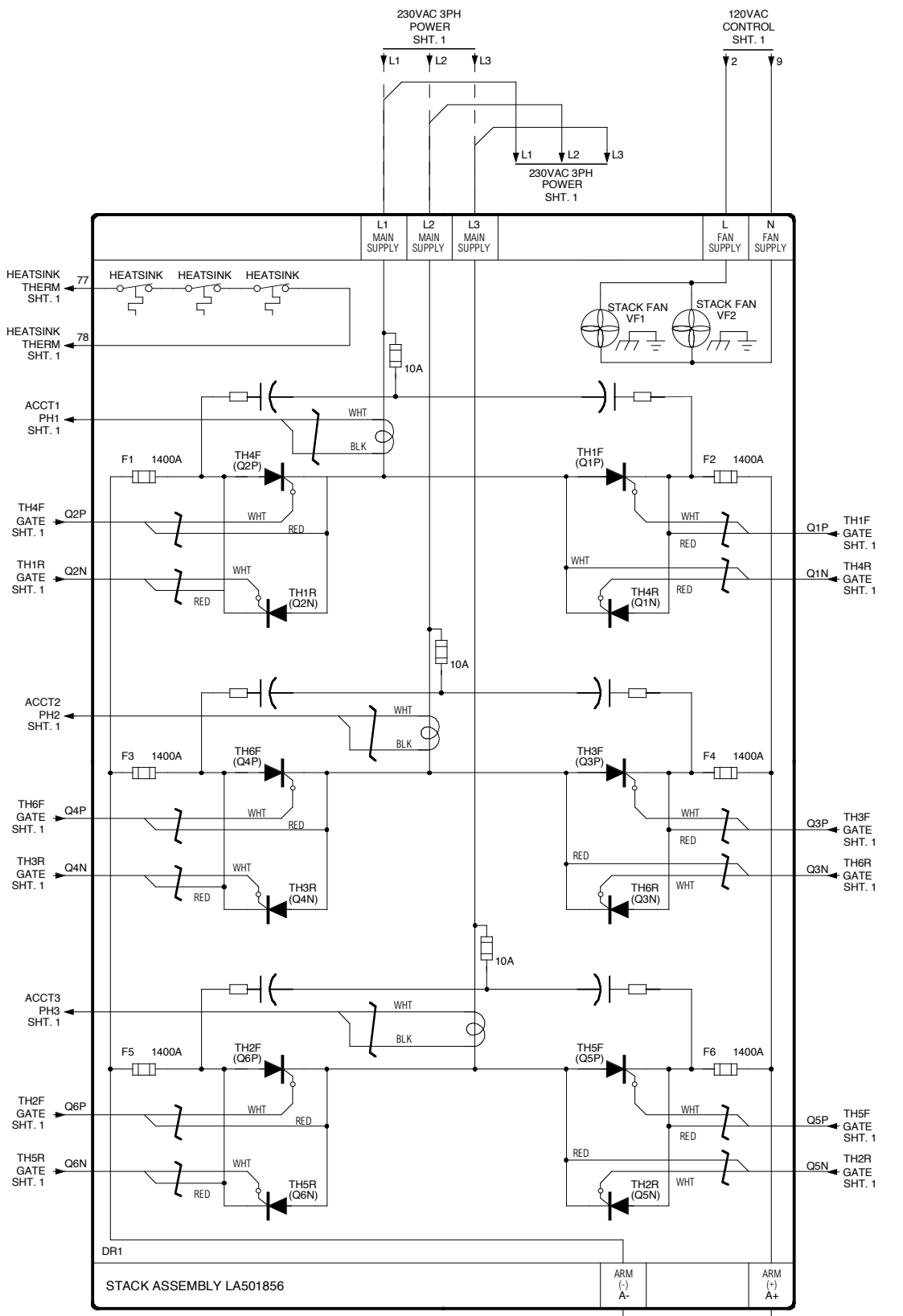
4

3

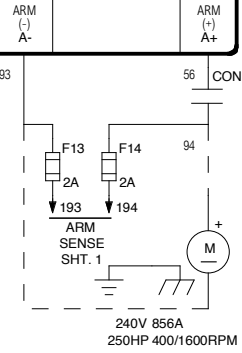
2

1

A B C D



STACK ASSEMBLY LA501856



DRN.	ENGINEER	ENGINEER	ENGINEER	ENGINEER
DESIGN	SCALE	DO NOT SCALE	PRE	OF
ANY CUSTOMER	SIZE	SCALE	2	2
SCR STACK	DRIVE PANEL CIRCUIT DIAGRAM	950A DC REGENERATIVE DRIVE PANEL	2	4
CUST.	DIST.	P.O.	2	2
SHT. TITLE	DWG. TYPE	JOB TITLE	JOB NO.	DWG. NO.
DRIVE PANEL CIRCUIT DIAGRAM	DRIVE PANEL CIRCUIT DIAGRAM	950A DC REGENERATIVE DRIVE PANEL	N/A	A
LOCATION	LOCATION	LOCATION	PRE	2
			2	2

Bardac
 40 Log Circle, Stevensville, MD 21666
 Phone (410) 604-3400, Fax: (410) 604-3500
 Email: info@bardac.com

tom: engr/cad/bnorm/asz

Bardac | | | | |
drives ' | | | | |

Bardac Corporation
40 Log Canoe Circle
Stevensville, MD 21666 USA
Phone: (410)604-3400 Fax: (410)604-3500
www.bardac.com